Hellcat-14 MS TGL

SCHEMATIC DIAGRAM

2020-10-12 (REV 1.0) (REV A00)

DY : None Installed

UMA: Unified Memory Architecture
OPS: Optimal Playable Settings

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Title	Cover Page	
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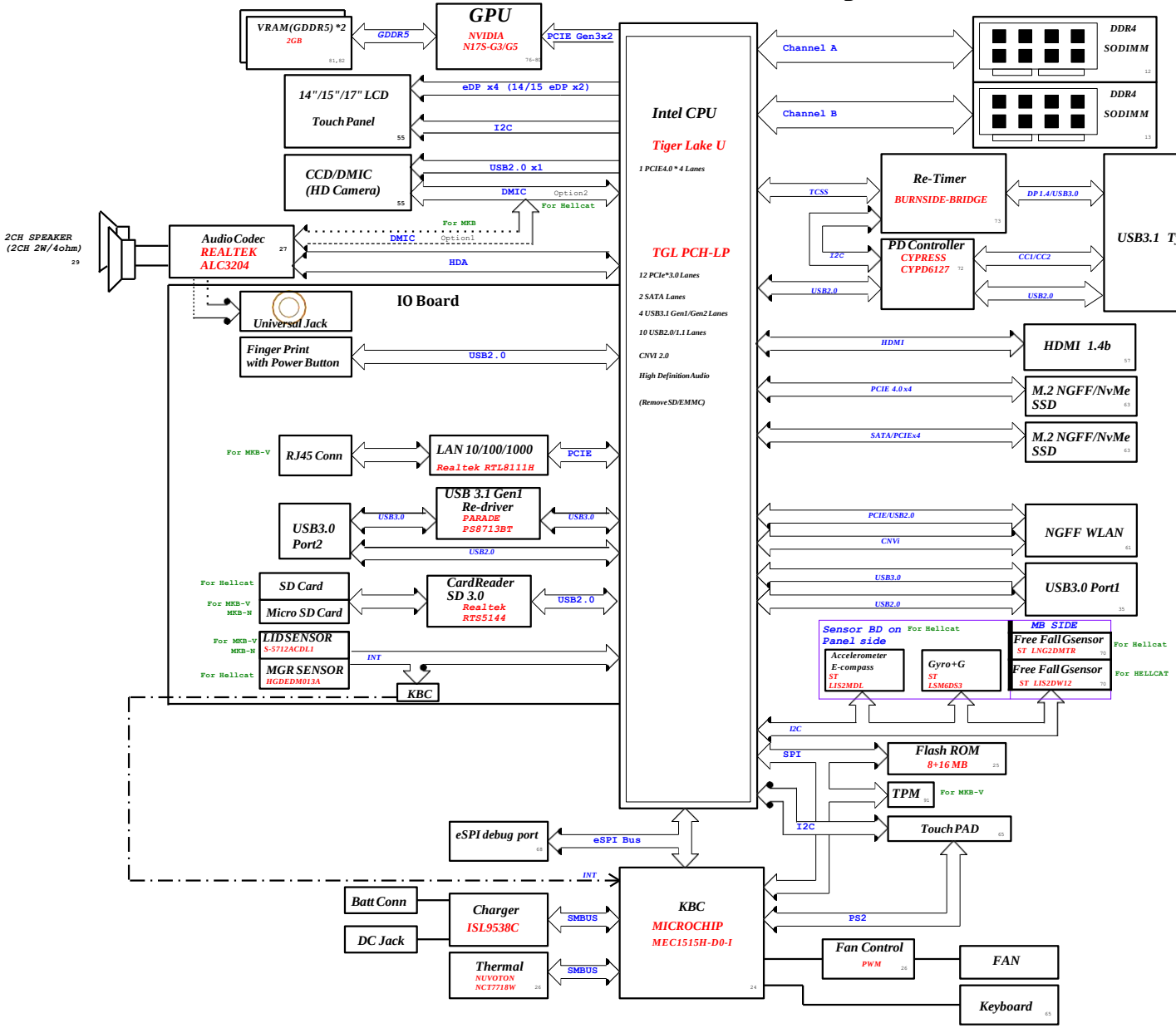
HellCat TGL Block Diagram



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Title: Block Diagram

Size: Document Number: HELLCAT_TGL — Rev: A00

Custom

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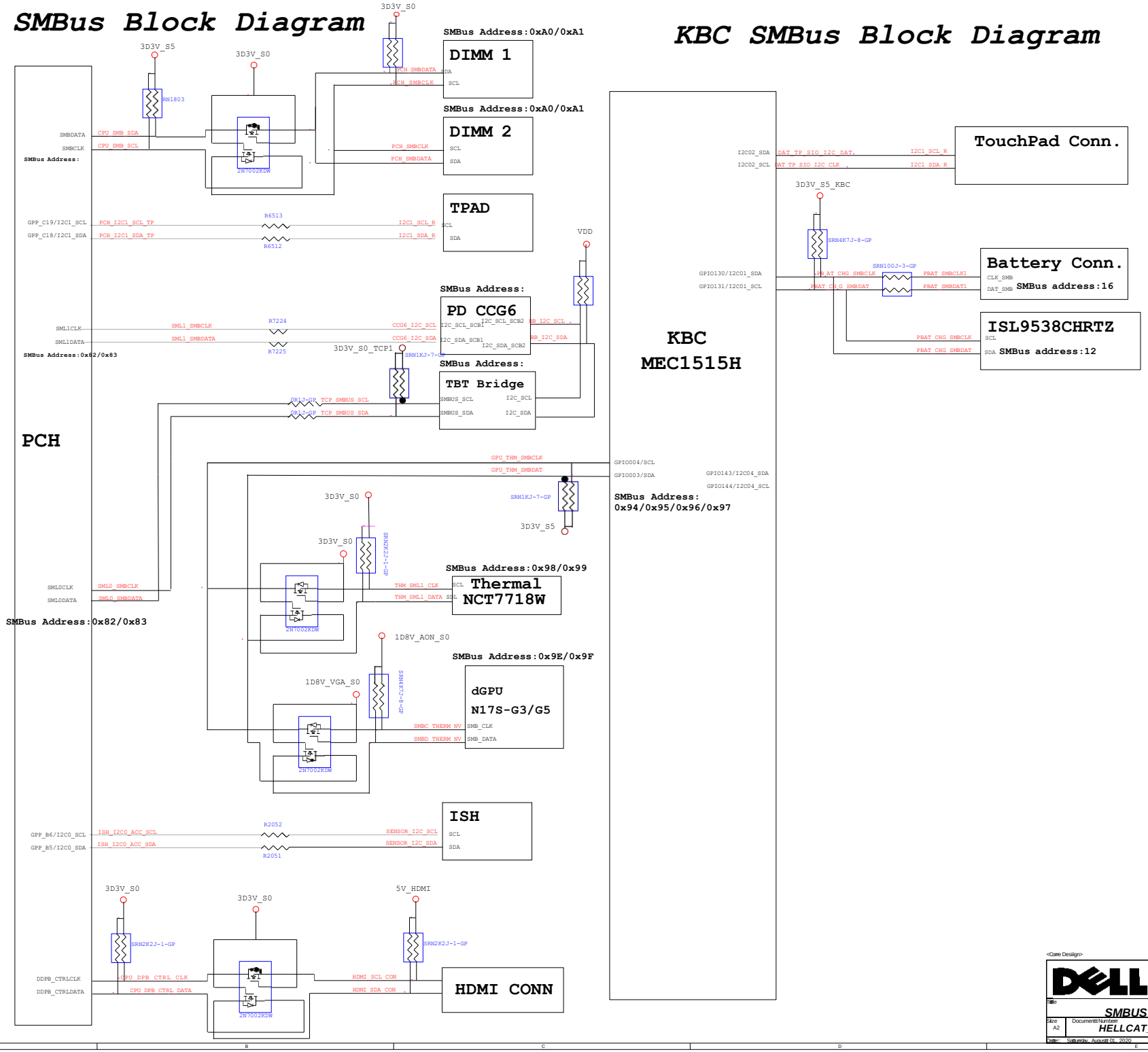
PCH SMBus Block Diagram

KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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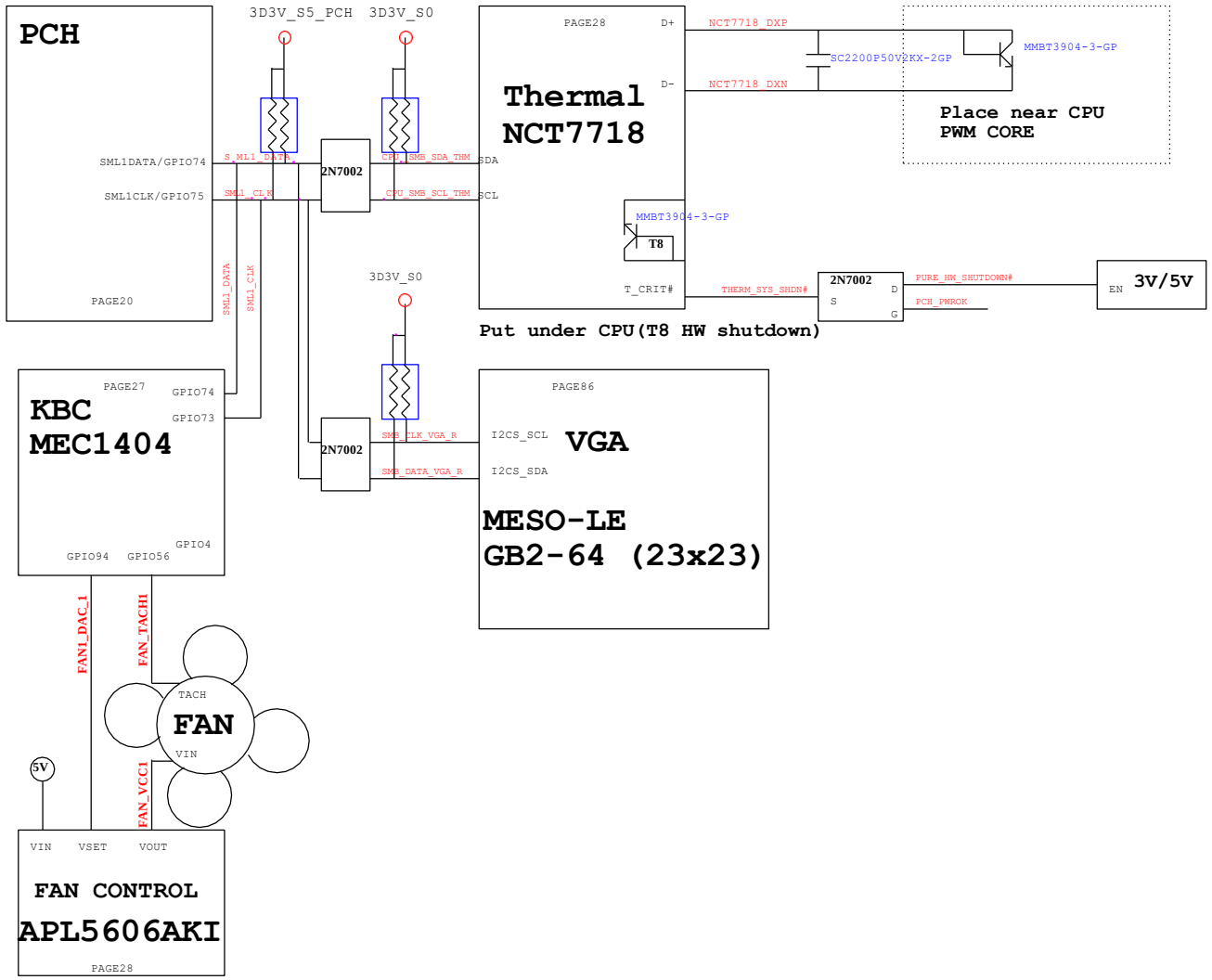
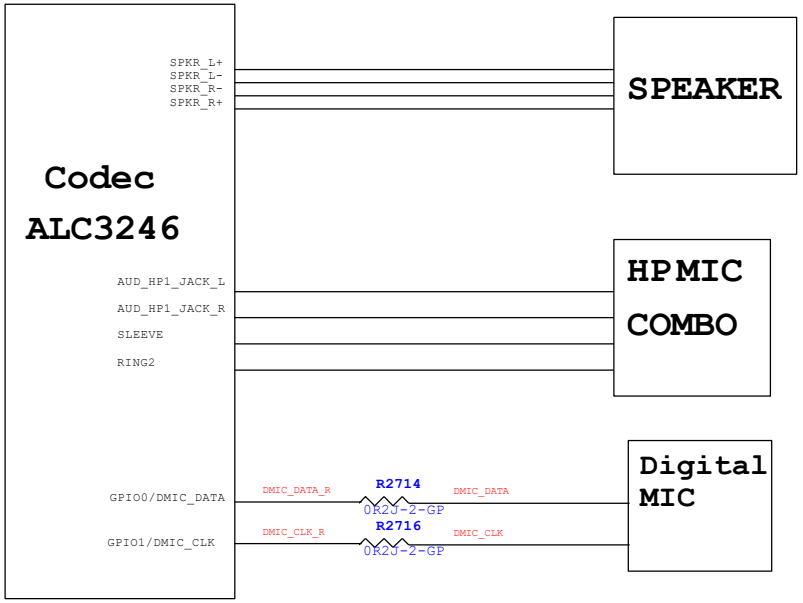
Thermal Block Diagram



Audio Block Diagram



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Title: *Thermal/Audio Block Diagram*

Size: Custom | Document Number: *HELLCAT_TGL* | Rev: *A00*

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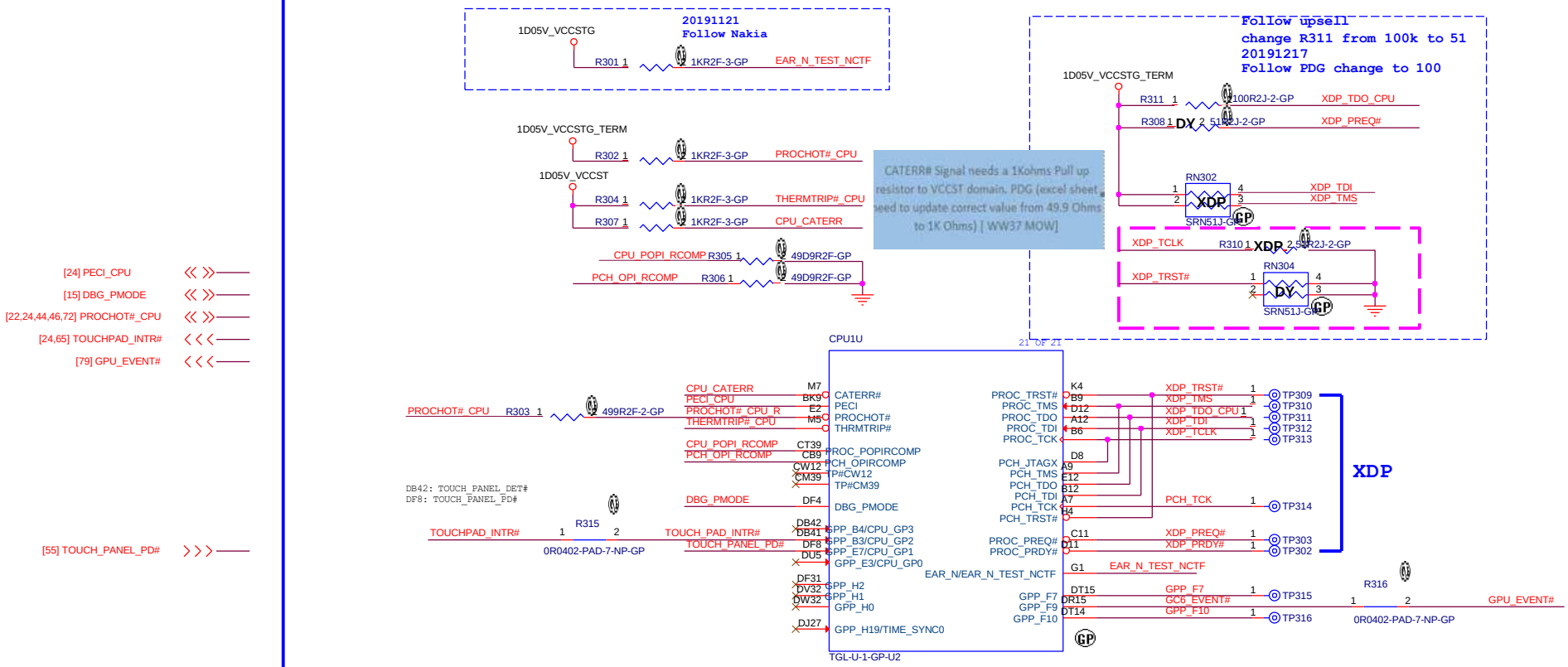

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Title: **CPU (THML/JTAG)**

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eDP

[55] eDP_TX_CPU_N0
[55] eDP_TX_CPU_P0
[55] eDP_TX_CPU_N1
[55] eDP_TX_CPU_P1
[55] eDP_TX_CPU_N2
[55] eDP_TX_CPU_P2
[55] eDP_TX_CPU_N3
[55] eDP_TX_CPU_P3
[55] eDP_AUX_CPU_N
[55] eDP_AUX_CPU_P
[55] EDP_HPD
[24] L_BKLT_EN
[55] eDP_VDD_EN
[55] L_BKLT_CTRL

HDMI

[57] HDMI_DDI_TX_P3
[57] HDMI_DDI_TX_N3
[57] HDMI_DDI_TX_P0
[57] HDMI_DDI_TX_N0
[57] HDMI_DDI_TX_P1
[57] HDMI_DDI_TX_N1
[57] HDMI_DDI_TX_P2
[57] HDMI_DDI_TX_N2

[57] CPU_DPB_CTRL_CLK
[57] CPU_DPB_CTRL_DATA

[57] CPU_DISP_HPDB

TBT

[71] USB1_TCSS_TX_N0
[71] USB1_TCSS_TX_P0
[71] USB1_TCSS_TX_N1
[71] USB1_TCSS_TX_P1
[71] USB1_TCSS_RX_N0
[71] USB1_TCSS_RX_P0
[71] USB1_TCSS_RX_N1
[71] USB1_TCSS_RX_P1

[71] TBT_LSX0_TXD
[15,71] TBT_LSX0_RXD

[71] USB1_TCSS_AUX_P
[71] USB1_TCSS_AUX_N

[72] SOC_OC_FAULT

Other

[15] GPP_E21
[15] GPP_D12
[15] GPP_D10
[65] KB_DET#

USB3.2 Type-A Port2 (IO)

[66] USB_OC1#

CPU1A

1 OF 21

eDP_TX_CPU_P3 AC2 DDIA_TXP3
eDP_TX_CPU_N3 AC1 DDIA_TXN3
eDP_TX_CPU_P2 AD2 DDIA_TXP2
eDP_TX_CPU_N2 AD1 DDIA_TXN2
eDP_TX_CPU_P1 AF1 DDIA_TXP1
eDP_TX_CPU_N1 AF2 DDIA_TXN1
eDP_TX_CPU_P0 AG2 DDIA_TXP0
eDP_TX_CPU_N0 AG1 DDIA_TXN0
eDP_AUX_CPU_P AJ2 DDIA_AUX_P
eDP_AUX_CPU_N AJ1 DDIA_AUX_N

TP401 1 GPP_E23 DN4 DT6 GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD
GPP_E23/DDPA_CTRLDATA
EDP_HPD DR5 GPP_E14/DDSP_HPDA/DISP_MISCA

HDMI_DDI_TX_P3 T12 DDIB_TXP3
HDMI_DDI_TX_N3 T11 DDIB_TXN3
HDMI_DDI_TX_P0 Y11 DDIB_TXP2
HDMI_DDI_TX_N0 Y9 DDIB_TXN2
HDMI_DDI_TX_P1 T9 DDIB_TXP1
HDMI_DDI_TX_N1 P9 DDIB_TXN1
HDMI_DDI_TX_P2 V11 DDIB_TXP0
HDMI_DDI_TX_N2 V9 DDIB_TXN0
AB9 DDIB_AUX_P
AD9 DDIB_AUX_N
CPU_DPB_CTRL_CLK DM29 GPP_H16/DDPB_CTRLCLK/PCIE_LNK_DOWN
CPU_DPB_CTRL_DATA DK27 GPP_H17/DDPB_CTRLDATA
CPU_DISP_HPDB DG43 GPP_A18/DDSP_HPDB/DISP_MISCB/I2S4_RXD

20191211 for TBT
KB_DET# DG47 DJ47 GPP_A21/DDPC_CTRLCLK/I2S5_TXD
GPP_A22/DDPC_CTRLDATA/I2S5_RXD

TBT_LSX0_TXD DU8 GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD
TBT_LSX0_RXD DV8 GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD

GPP_E21 DF6 DD6 GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD
GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD

GPP_D10 DN23 DM23 GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK

GPP_D12 DK23 DN21 GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO
GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI

CPU_DISP_HPD1_R DF43 DF45 GPP_A17/DISP_MISCC/I2S4_TXD
GPP_A19/DDSP_HPD1/DISP_MISC1/I2S5_SCLK
DF47 GPP_A20/DDSP_HPD2/DISP_MISC2/I2S5_SFRM

20191211 follow vendor request
USB_OC1# DH52 GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1
SOC_OC_FAULT DK45 GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK

eDP_VDD_EN DM8 EDP_VDDEN
L_BKLT_EN DN8 EDP_BKLTEN
L_BKLT_CTRL DG10 EDP_BKLTCTL

TGL-U-1-GP-U2

20191211 for TBT

TCP0_TXRX_P1 AY2 USB1_TCSS_RX_P1
TCP0_TXRX_N1 AY1 USB1_TCSS_RX_N1
TCP0_TXRX_P0 BB1 USB1_TCSS_RX_P0
TCP0_TXRX_N0 BB2 USB1_TCSS_RX_N0
TCP0_TX_P1 AM5 USB1_TCSS_TX_P1
TCP0_TX_N1 AM7 USB1_TCSS_TX_N1
TCP0_TX_P0 AT7 USB1_TCSS_TX_P0
TCP0_TX_N0 AT5 USB1_TCSS_TX_N0 AP7
TCP0_AUX_P USB1_TCSS_AUX_P AP5
TCP0_AUX_N USB1_TCSS_AUX_N

TCP1_TXRX_P1 AT2
TCP1_TXRX_N1 AT1
TCP1_TXRX_P0 AU1
TCP1_TXRX_N0 AU2
TCP1_TX_P1 AD5
TCP1_TX_N1 AD7
TCP1_TX_P0 AH7
TCP1_TX_N0 AH5
TCP1_AUX_P AF7
TCP1_AUX_N AF5

TCP2_TXRX_P1 BF1
TCP2_TXRX_N1 BF2
TCP2_TXRX_P0 BE2
TCP2_TXRX_N0 BE1
TCP2_TX_P1 BD7
TCP2_TX_N1 BD5
TCP2_TX_P0 AY5
TCP2_TX_N0 AY7
TCP2_AUX_P BB5
TCP2_AUX_N BB7

TCP3_TXRX_P1 BK1
TCP3_TXRX_N1 BK2
TCP3_TXRX_P0 BJ2
TCP3_TXRX_N0 BJ1
TCP3_TX_P1 BM7
TCP3_TX_N1 BM5
TCP3_TX_P0 BH5
TCP3_TX_N0 BH7
TCP3_AUX_P BK5
TCP3_AUX_N BK7

TC_RCOMP_P AN2 TCSS_RCOMP_P
TC_RCOMP_N AN1 TCSS_RCOMP_N R402 1 150R2F-1-GP
DSI_DE_TE_2 M8
DDI_RCOMP AB1 DISP_RCOMP R401 1 150R2F-1-GP
DISP_UTILS/DSI_DE_TE_1 CE4

TBT

20191211 for TBT

DN4: WWAN_GPO_PERST#
DT6: WWAN_CARD_PWR_OFF#
DG47: 3.3V_CAM_EN
DF6: TBT_LSX1_TXD
DN23: SENSOR_DB_DET#
DD6: TBT_LSX1_RXD
DK23: CPU_DDP4_CTRL_CLK
DN21: CPU_DDP4_CTRL_DATA
DF47: CPU_DISP_HPD2
DH52: USB_OC1#
DK45: CPU_DISP_HPD4

CPU_DISP_HPD1_R R403 1 DY 100KR2J-1-GP

20191129 layout Request

3D3V_S0 RN402 2 1 4 CPU_DPB_CTRL_CLK CPU_DPB_CTRL_DATA
SRN2K2J-1-GP
R419 1 2 10KR2J-3-GP KB_DET#

3D3V_S5_VCCPRIM 20191211 Remove R422
R421 1 2 USB_OC1#
10KR2J-3-GP
20191224 Follow Internal review

Add RTC Gen 9 reset circuit_20170814
leakage issue 20191224 Follow Internal review

3D3V_S5_VCCPRIM
R406 10KR2J-3-GP RTC_RST
3D3V_S5_VCCPRIM
R405 10KR2J-3-GP RTC_RST
Q401
CPU_DISP_HPD1_R
CPU_DISP_HPD1_P
RTC_RST
2N7002KDW-1-GP

75.27002.F7C
2nd = 075.27002.0E7C
3rd = 075.67002.007C
4th = 075.07002.0A7C

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Title: CPU (DDI/EDP/TBT/TPC/)

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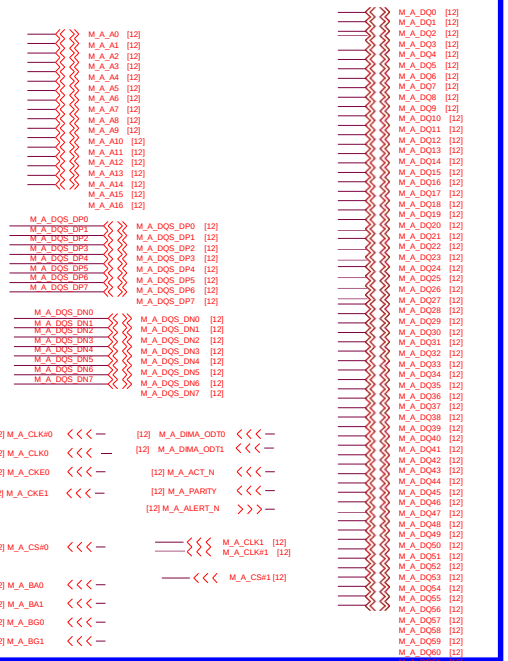
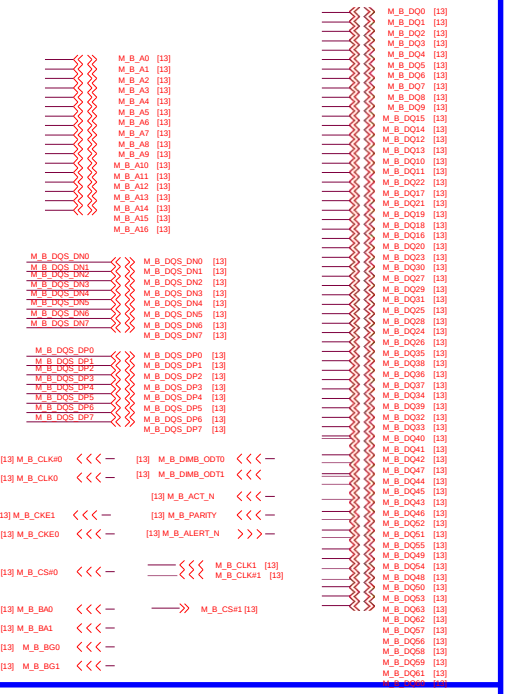
DDR4 ball type: Non-Interleaved Type

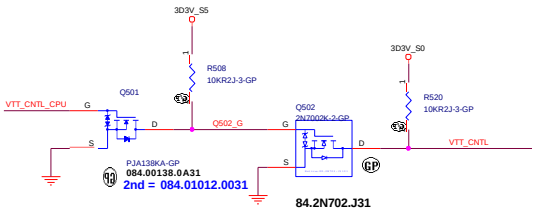
Channel A



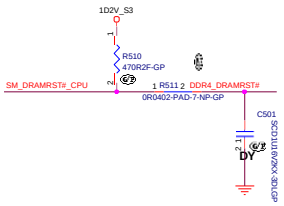
Channel B



[12] V_SM_VREF_CNTA
[13] V_SM_VREF_CNTB
[51] VTT_CNTL
[12,13] DDR4_DRAMRST#



84.2N702.J31
2ND = 084.27002.0N31
3rd =084.27002.0L31
4th = 084.07002.0C31



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Title: **CPU (DDR)**

Size	Document Number	Rev
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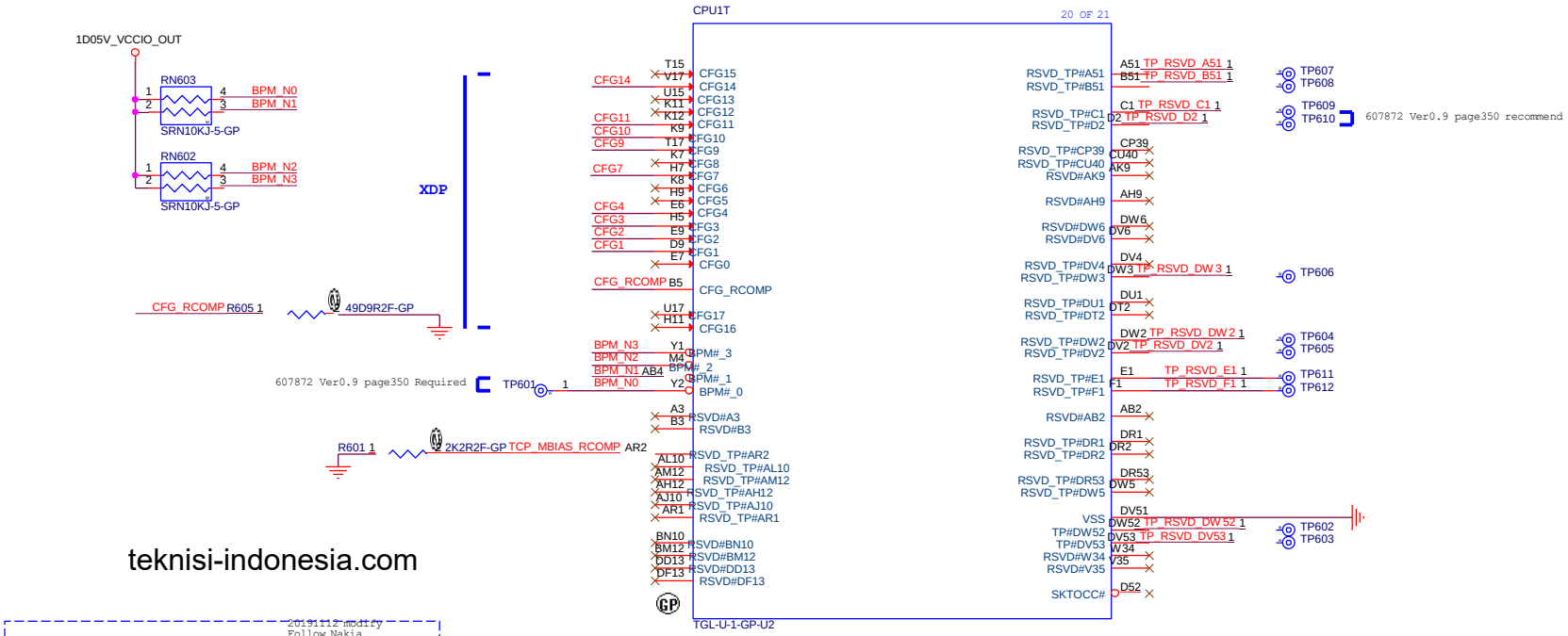

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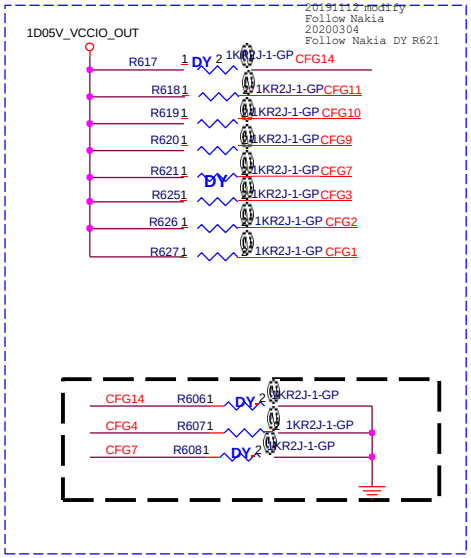

607872 Ver0.9 page350 Required

CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall	Pull-up to VCCSTG	1K ohm
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

Bifurcation	Link Width	CFG Signals	Lanes			
	0:6:0	CFG [14]	0	1	2	3
1x4	x4	0	0	1	2	3
1x4 **Reversed**	x4	1	3	2	1	0

Notes:
1. PCIe* Port60 is a single x4 port without bifurcation capabilities, thus bifurcation pin straps are not applicable.

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Title: ***CPU (CFG/IST)***

Size: A3 | Document Number: ***HELLCAT_TGL*** | Rev: ***A00***

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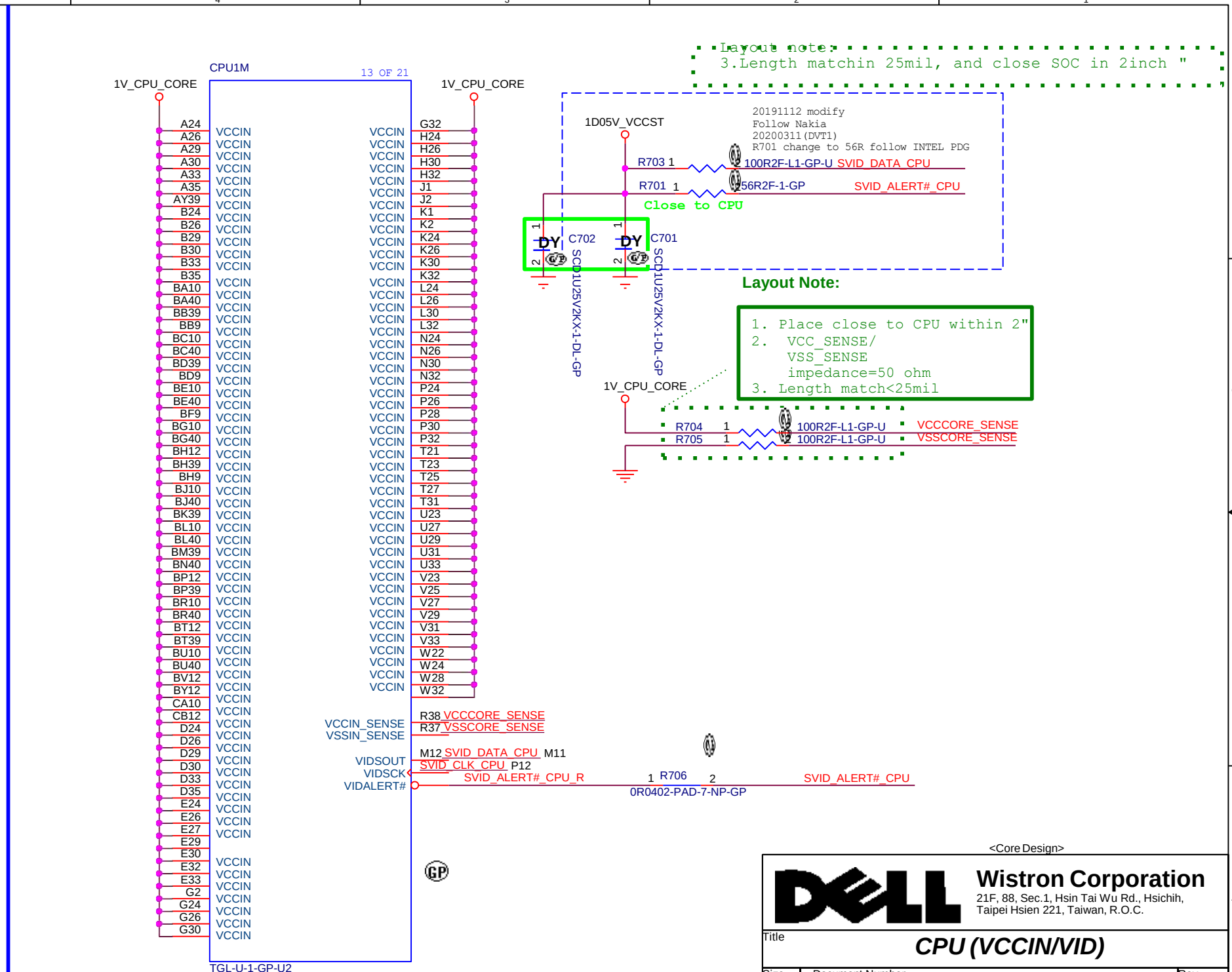

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Title: **CPU (VCCIN/VID)**

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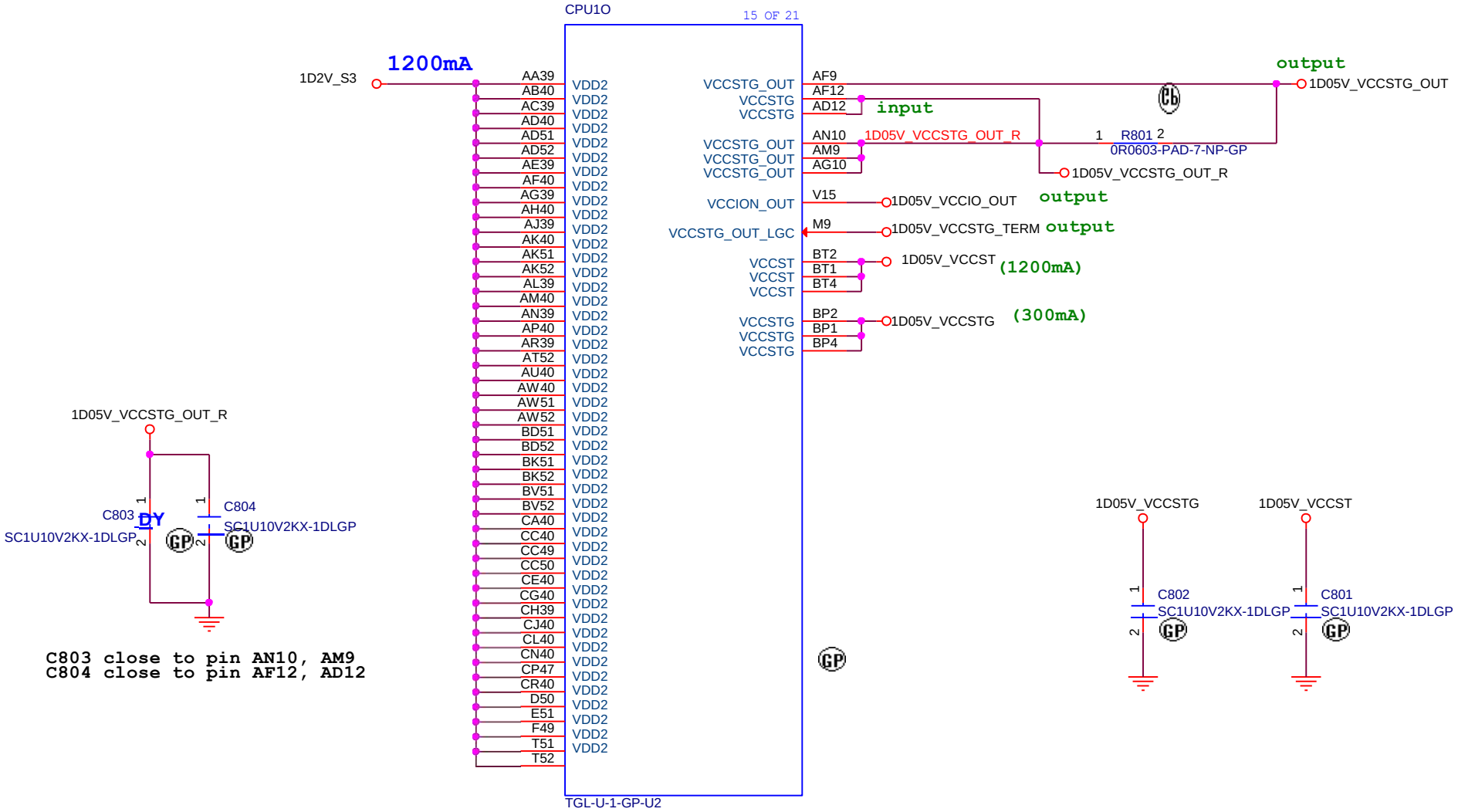
Main Func = CPU



C803 close to pin AN10, AM9
C804 close to pin AF12, AD12

Lack of VCCPLL_OC / VCC1P8A / VCCPLL

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Title: CPU (VDDQ/VCC/VCCST/VCCSTG)

Size	Document Number	Rev
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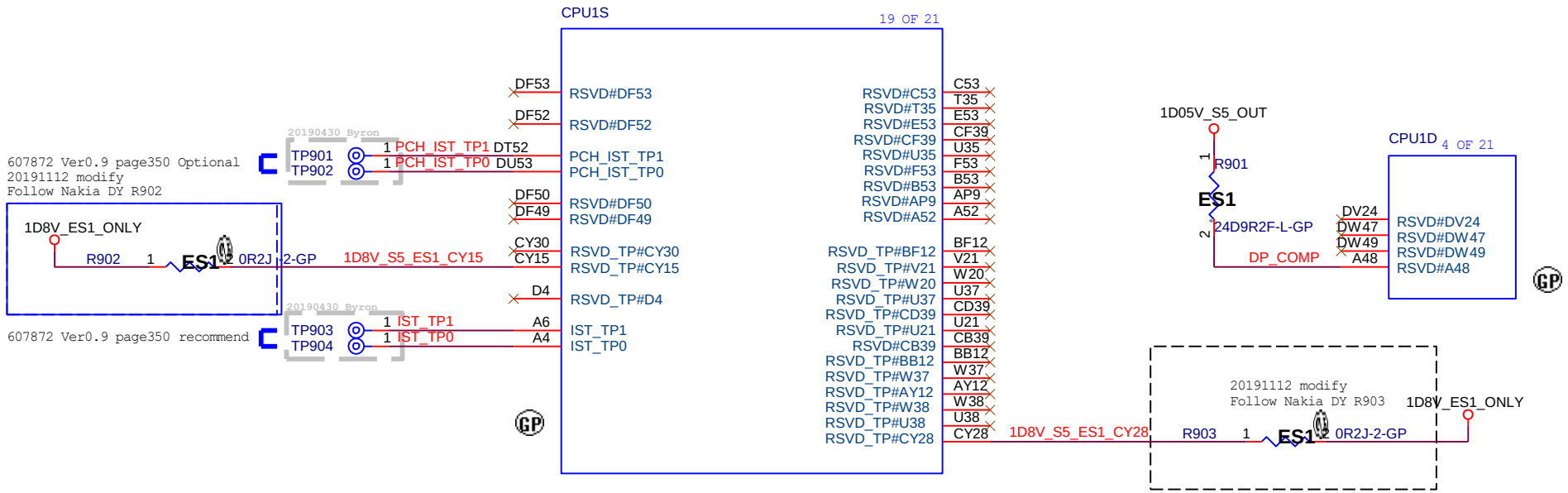

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Title	CPU (RSVD)	
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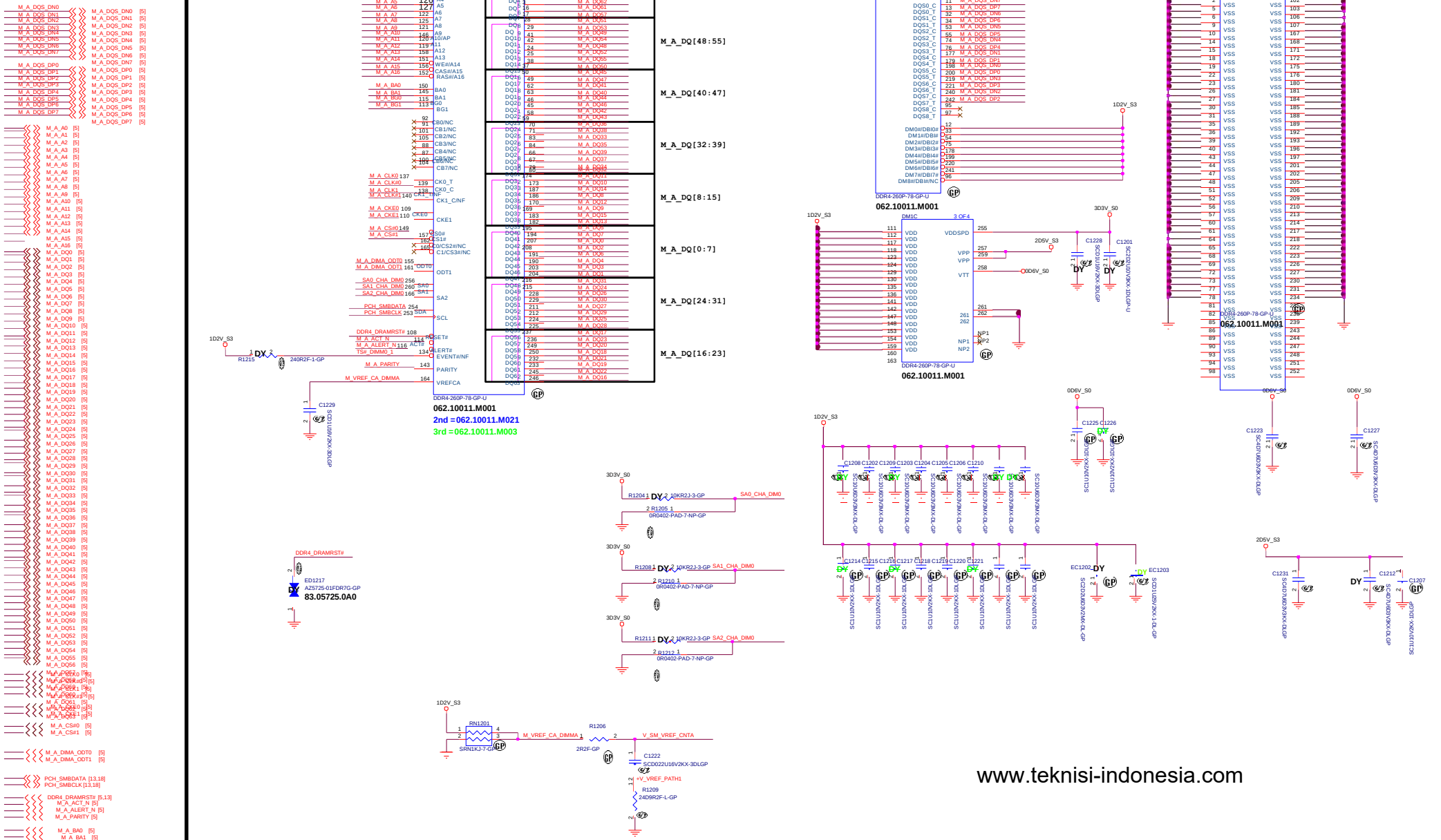
Main Func = MEMORY



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Title: DDR3-SODIMM1

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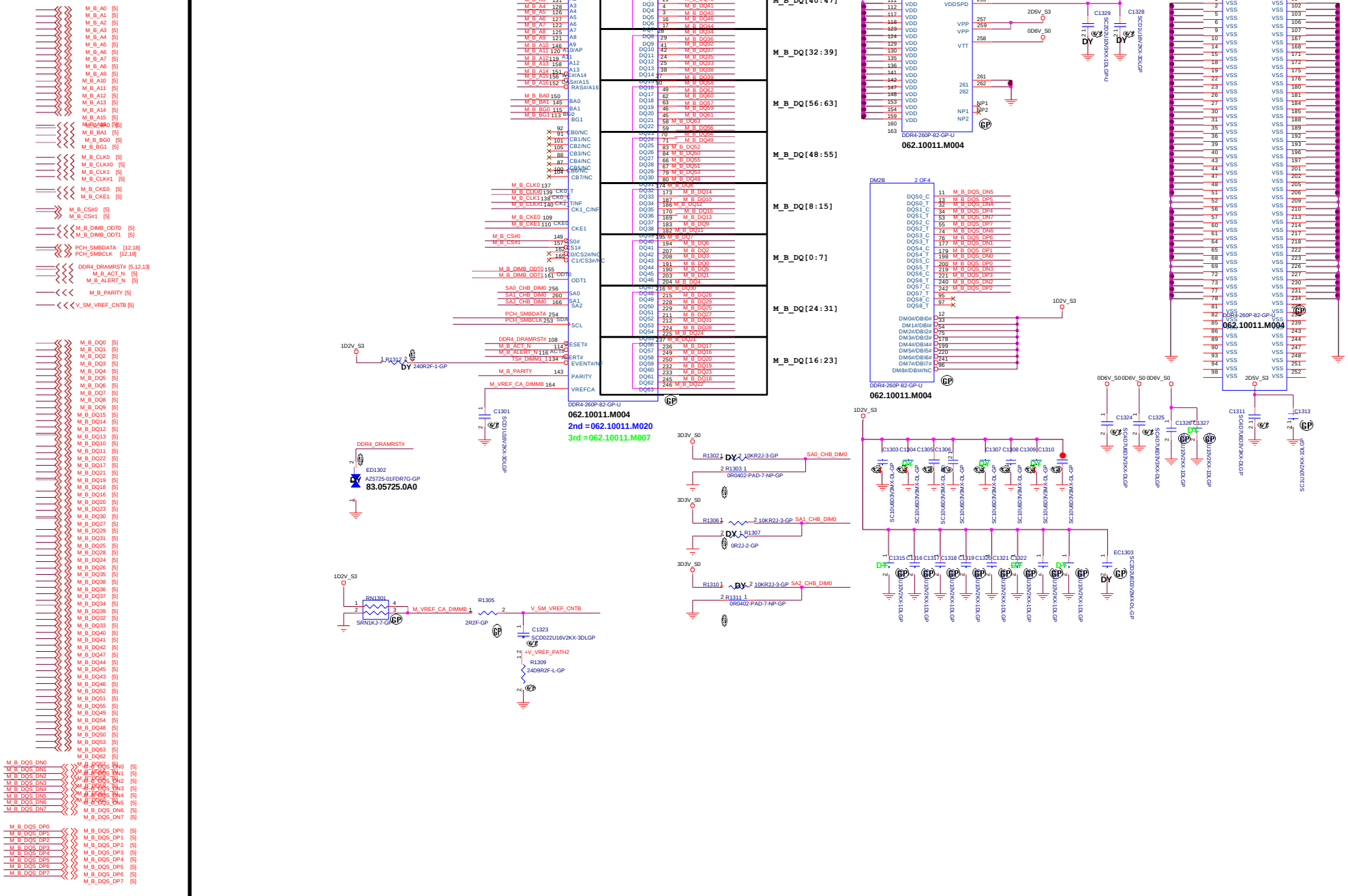
Main Func = MEMORY



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Title: ***DDR3-SODIMM1***

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[18,24,25,91] SPI_SI_ROM
[18,24,25] SPI_WP_ROM
[18,24,25] SPI_HOLD_ROM

[21] CNV_RGI_DT
[18] SML0_ALERT#
[18] GPP_E6
[19] HDA_SDO
[4,71] TBT_LSX0_RXD
[4] GPP_D10
[3] DBG_PMODE
[4] GPP_D12
[4] GPP_E21
[18] GPP_E10
[18] GPP_E11

GPIO	GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_F2)
Schematic	=20K PD= 3D3V_S5 R1501 DY 4K7R2J-2-GP SML0_ALERT# R1502 DY 20K5R2F-GP	=NO INTERNAL= 3D3V_S5 R1503 4K7R2J-2-GP BOOT_HALT SPI_SI_ROM Close to U2501 R1511 20200221 (DVT1) DY Change to 4.7k follow CRB 4K7R2J-2-GP	=NO INTERNAL= 3D3V_S5 R1504 100KR2J-1-GP GPP_E6 R1512 DY 4K7R2J-2-GP	=20K PD=	=NO INTERNAL= 3D3V_SPI R1506 100KR2J-1-GP SPI_WP_ROM Close to U2501 R1514 DY 4K7R2J-2-GP CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	=20K PD= * PH as VCCPGPPR 1D8V_GPPR_S5 R1509 Follow Nakia using 1.8V GPPR DY 4K7R2J-2-GP ME_UNLOCK 1 R1515 2 HDA_SDO 0R0402-PAD-7-NP-GP	=NO INTERNAL= 1D8V_S5 R1507 100KR2J-1-GP CNV_RGI_DT R1516 DY 4K7R2J-2-GP
High	default						
Low	=default=						

GPIO	TBT LSX VCCIO conf.#0	TBT LSX VCCIO conf.#1	TBT LSX VCCIO conf.#2	TBT LSX VCCIO conf.#3	A0		GPP_E10	GPP_E11
Schematic	E19 =NO INTERNAL= 3D3V_S5 R1518 DY 4K7R2J-2-GP TBT_LSX0_RXD R1521 sky 0329 20KR2J-L2-GP	E21 =NO INTERNAL= 3D3V_S5 R1519 DY 4K7R2J-2-GP GPP_E21 R1522 sky 0329 20KR2J-L2-GP	D10 =NO INTERNAL= 3D3V_S5 R1520 DY 4K7R2J-2-GP GPP_D10 R1523 sky 0329 20KR2J-L2-GP	D12 =NO INTERNAL= 3D3V_S5 R1524 DY 4K7R2J-2-GP GPP_D12 R1525 sky 0329 20KR2J-L2-GP	=NO INTERNAL= 3D3V_S5 R1526 100KR2J-1-GP SPI_HOLD_ROM Close to U2501 DY R1527 100KR2J-1-GP	=20K PU= 1D05V_S5_OUT R1528 20191211 Always stuff Follow Nakia 1KR2F-3-GP DBG_PMODE R1529 DY 1KR2F-3-GP	1D8V_S5 R1531 20KR2J-L2-GP GPP_E10	1D8V_S5 R1530 20KR2J-L2-GP GPP_E11
High								
Low								

Original Ref.

GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK	M.2 CNVI MODES	TBT LSX #0
ESPI OR EC LESS HIGH: ESPI IS DISABLED LOW: ESPI SELECTED WEAK INTERNAL PD 20K	BOOT HALT HIGH - DISABLED LOW- ENABLED NO INTERNAL PU/PD	JTAG ODT DISABLE LOW: JTAG ODT DISABLED HIGH: JTAG ODT ENABLED NO INTERNAL PU/PD	CPUNSSC CLOCK FREQ HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL) LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT) WEAK INTERNAL PD 20K	CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	FLASH DESCRIPTOR SECURITY OVERRIDE HIGH: OVERRIDEN LOW: SECURITY MEASURES NOT OVERRIDEN WEAK INTERNAL PD 20K	M.2 CNVI MODES LOW-> INTEGRATED CNVI ENABLE HIGH-> INTEGRATED CNVI DISABLE NO INTERNAL PU/PD	TBT LSX #0 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD
TBT LSX #1	**TBT LSX #2**	**TBT LSX #3**	**A0**	**GPP_E10**	**GPP_E11**		
TBT LSX #1 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #2 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #3 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	A0 PERSONALITY STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	RA RB	RA RB		

<Core Design>

Wistron Corporation
21F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)

Size: A2 | Document Number: HELLCAT_TGL | Rev: A00

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GPU

[76] GFX_PCIE_TX_P0
[76] GFX_PCIE_TX_N0
[76] GFX_PCIE_RX_P0
[76] GFX_PCIE_RX_N0

[76] GFX_PCIE_TX_P1
[76] GFX_PCIE_TX_N1
[76] GFX_PCIE_RX_P1
[76] GFX_PCIE_RX_N1

M.2 SSD1

[63] SSD_PCIE_TX_P0
[63] SSD_PCIE_TX_N0
[63] SSD_PCIE_RX_P0
[63] SSD_PCIE_RX_N0

[63] SSD_PCIE_TX_P1
[63] SSD_PCIE_TX_N1
[63] SSD_PCIE_RX_P1
[63] SSD_PCIE_RX_N1

[63] SSD_PCIE_TX_P2
[63] SSD_PCIE_TX_N2
[63] SSD_PCIE_RX_P2
[63] SSD_PCIE_RX_N2

[63] SSD_PCIE_TX_P3
[63] SSD_PCIE_TX_N3
[63] SSD_PCIE_RX_P3
[63] SSD_PCIE_RX_N3

M.2 SSD2

[63] SSD_PCIE_TX_P9
[63] SSD_PCIE_TX_N9
[63] SSD_PCIE_RX_N9
[63] SSD_PCIE_RX_P9

[63] SSD_PCIE_TX_P10
[63] SSD_PCIE_TX_N10
[63] SSD_PCIE_RX_P10
[63] SSD_PCIE_RX_N10

[63] SSD_PCIE_TX_P11
[63] SSD_PCIE_TX_N11
[63] SSD_PCIE_RX_P11
[63] SSD_PCIE_RX_N11

[63] SSD_PCIE_TX_P12
[63] SSD_PCIE_TX_N12
[63] SSD_PCIE_RX_P12
[63] SSD_PCIE_RX_N12

[63] M2_DEVSLP1
[63] M2_PEDET1

USB1

USB3.2 Type-A Port1 (MB)

[35] USB1_USB30_RX_N
[35] USB1_USB30_RX_P
[35] USB1_USB30_TX_N
[35] USB1_USB30_TX_P

[35] USB1_USB20_P
[35] USB1_USB20_N

[35] USB_OC0#

USB2

USB3.2 Type-A Port2 (IO)

[66] USB2_USB30_RX_N
[66] USB2_USB30_RX_P
[66] USB2_USB30_TX_N
[66] USB2_USB30_TX_P

[66] USB2_USB20_P
[66] USB2_USB20_N

Card Reader

[66] CARD1_USB20_P
[66] CARD1_USB20_N

Camera

[55] CCD_USB20_P
[55] CCD_USB20_N

Finger Print

[66] FP1_USB20_N
[66] FP1_USB20_P

TpyeC

[72] USB4_USB20_P
[72] USB4_USB20_N

[71,72] TBT_FORCE_PWR

PD

[17,71] PCH_TBT_PERST#

BT

[61] BT_USB20_P
[61] BT_USB20_N

WLAN

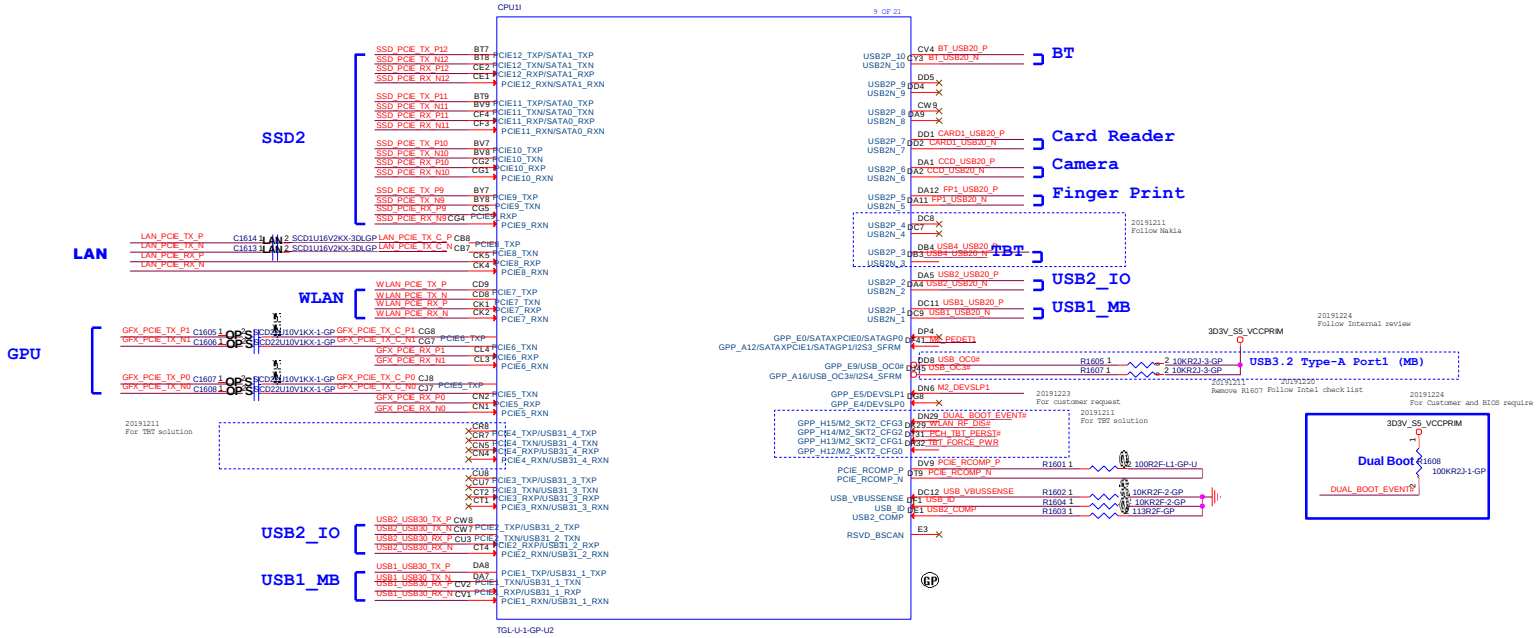
[61] WLAN_RF_DIS#

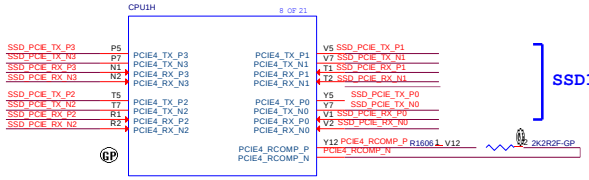
[61] WLAN_PCIE_RX_N
[61] WLAN_PCIE_RX_P
[61] WLAN_PCIE_TX_N
[61] WLAN_PCIE_TX_P

LAN

[66] LAN_PCIE_RX_N
[66] LAN_PCIE_RX_P
[66] LAN_PCIE_TX_N
[66] LAN_PCIE_TX_P

[24] DUAL_BOOT_EVENT#



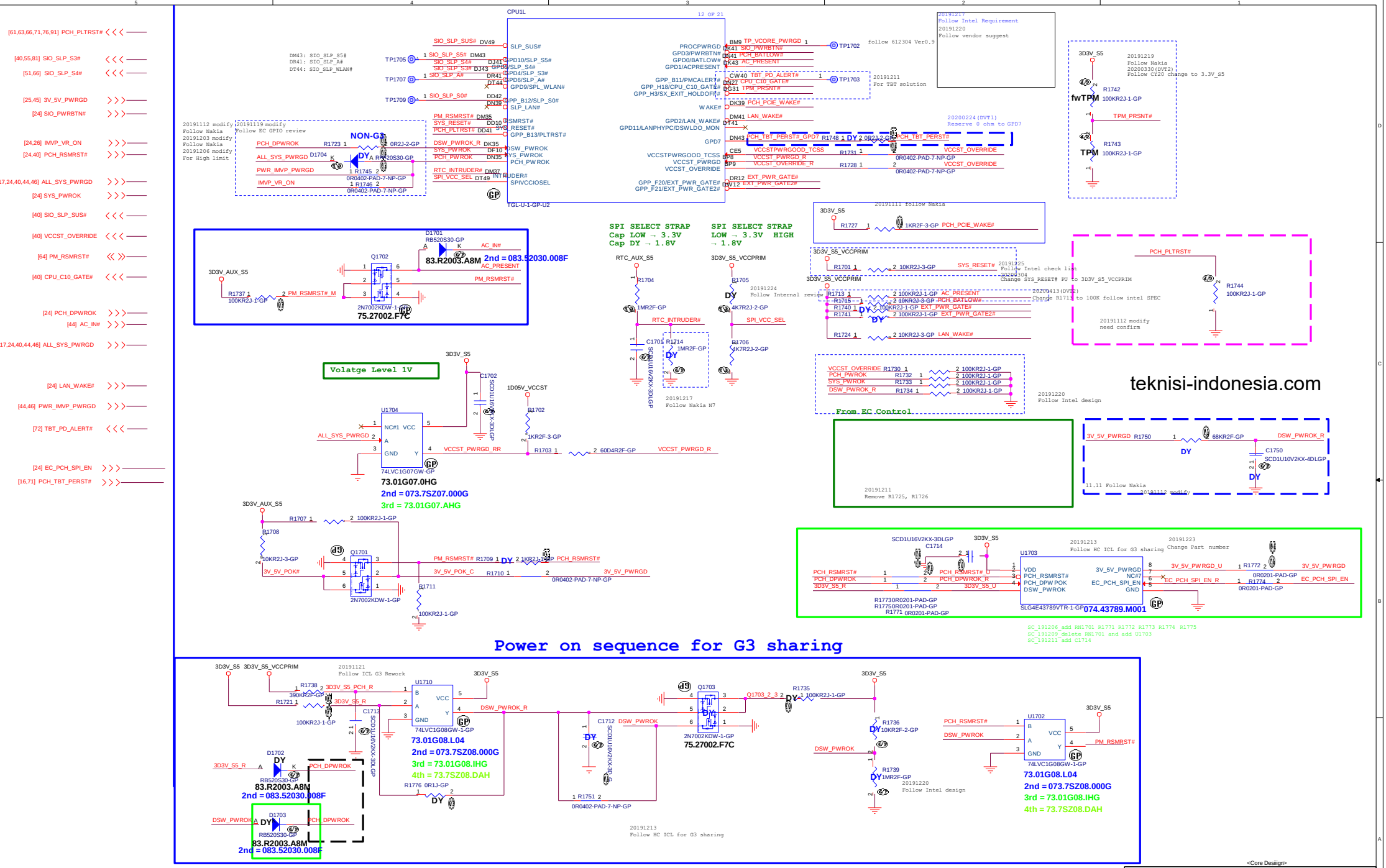


<Core Design>
Wistron Corporation
2F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB)

Size: A2 | Document Number: HELLCAT_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 16 of 105

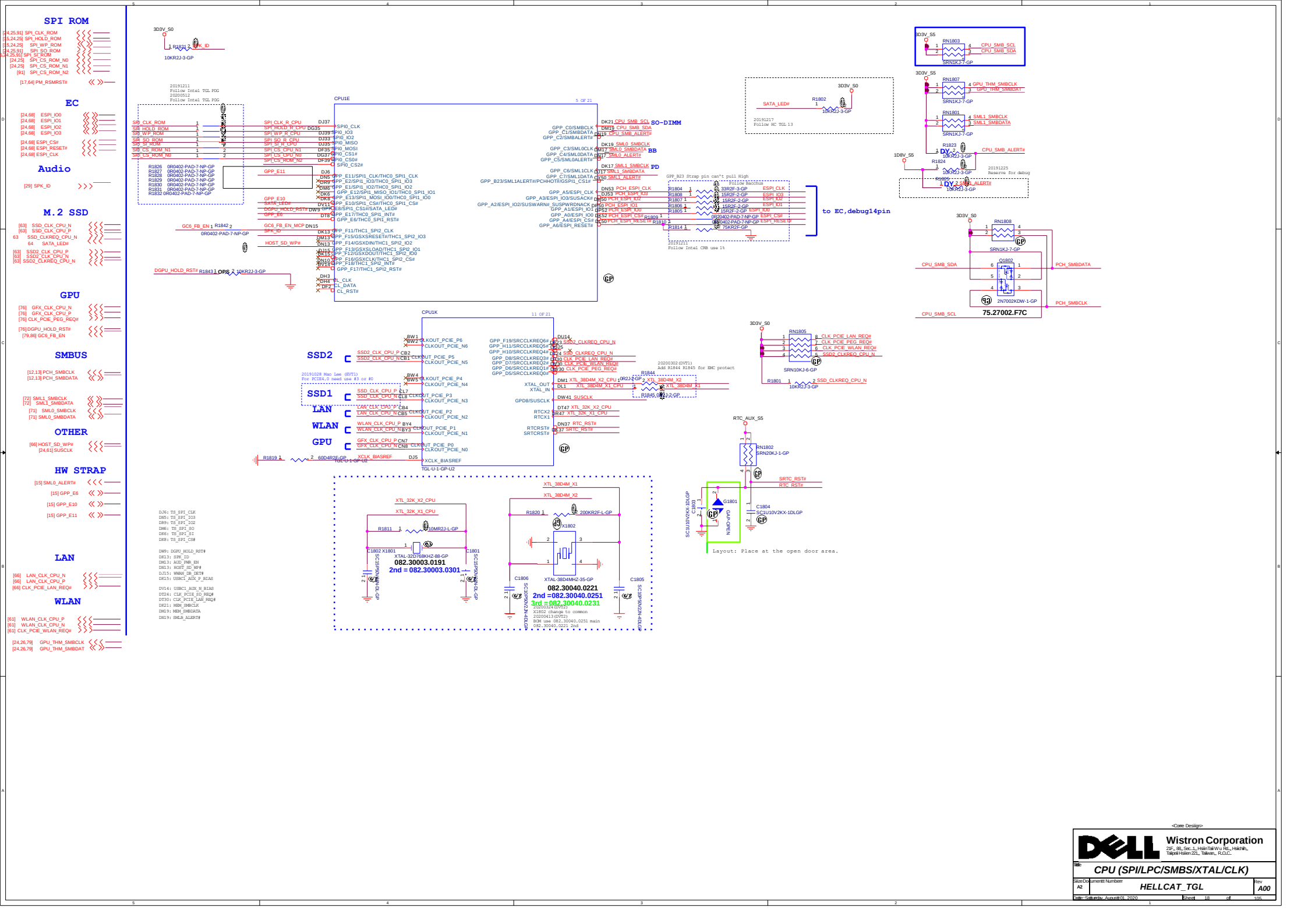


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PMU)

Size: Custom | Document Number: HELLCAT_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 17 of 105


SPI ROM
EC
Audio
M.2 SSD
GPU
SMBUS
OTHER
HW STRAP
LAN
WLAN
CPU1E
CPU1K
SO-DIMM
BB
PD
to EC,debug14pin
SSD2
SSD1
LAN
WLAN
GPU
75.27002.F7C
Wistron Corporation
CPU (SPI/LPC/SMBS/XTAL/CLK)
HELLCAT_TGL
A00
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Audio

[27] HDA_SYNC_CODEC
[27] HDA_BITCLK_CODEC
[27] HDA_SDOUT_CODEC
[27] HDA_SDIN0_CPU
[15] HDA_SDO
[55] DMIC_PCH_CLK_Q
[55] DMIC_PCH_DATA_Q

GPU

[24,85] DGPU_PWROK
[86] DGPU_PWR_EN

G SENSOR

[70] FFS_INT2

RTC

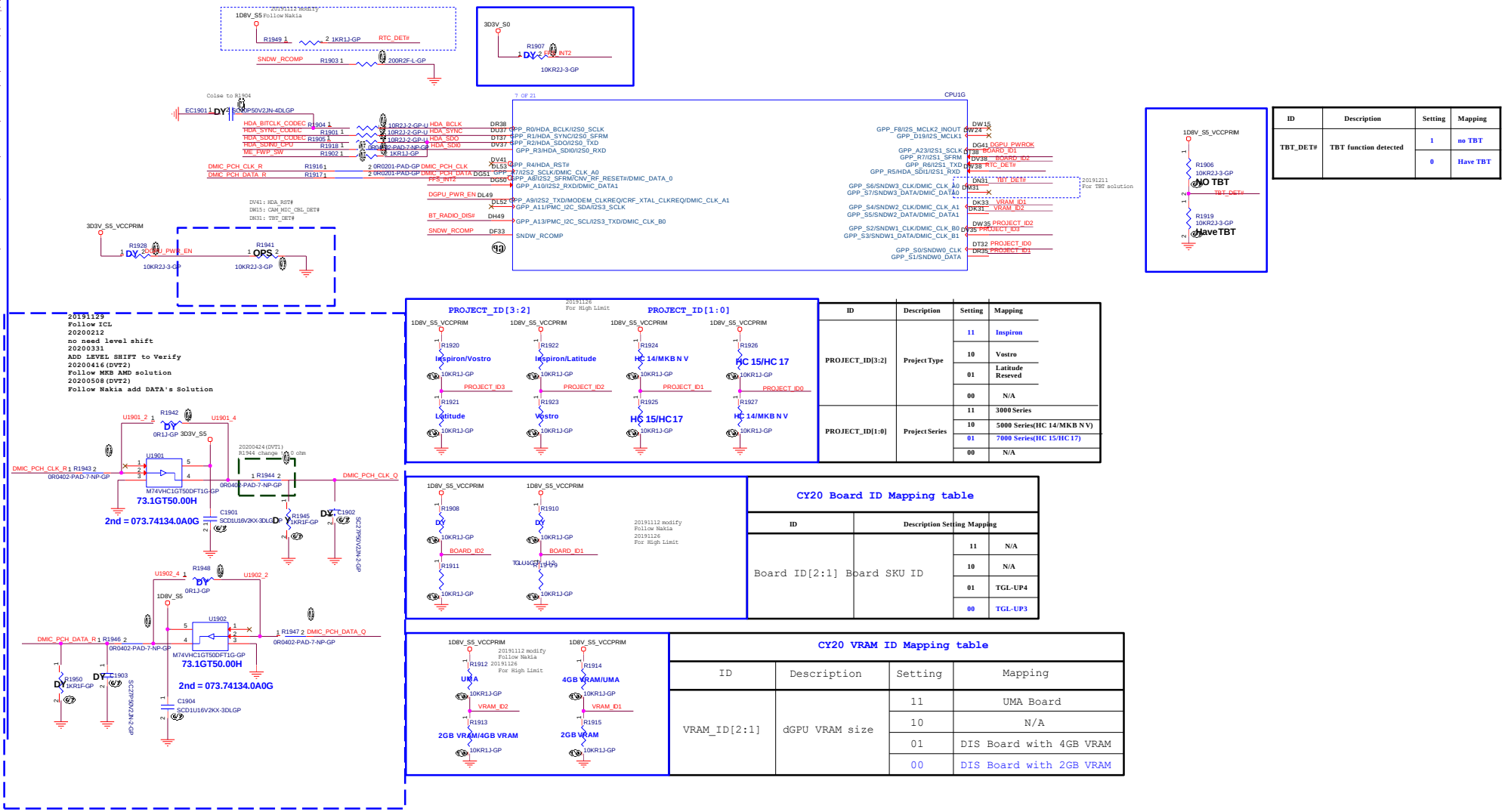
[25] RTC_DET#

BT

[61] BT_RADIO_DIS#

ME

[98] ME_FWP_SW



ID	Description	Setting	Mapping
TBT_DET#	TBT function detected	1	no TBT
		0	Have TBT

For SITP

20191129
Follow ICL
20200212
no need level shift
20200331
ADD LEVEL SHIFT to Verify
20200416 (DVT2)
Follow MKB AMD solution
20200508 (DVT2)
Follow Nakia add DATA's Solution

ID	Description	Setting	Mapping
PROJECT_ID[3:2]	Project Type	11	Inspiron
		10	Vostro
		01	Latitude Reseved
		00	N/A
PROJECT_ID[1:0]	Project Series	11	3000 Series
		10	5000 Series(HC 14/MKB N V)
		01	7000 Series(HC 15/HC 17)
		00	N/A

CY20 Board ID Mapping table			
ID	Description Setting Mapping		
Board ID[2:1]	Board SKU ID	11	N/A
		10	N/A
		01	TGL-UP4
		00	TGL-UP3

CY20 VRAM ID Mapping table			
ID	Description	Setting	Mapping
VRAM_ID[2:1]	dGPU VRAM size	11	UMA Board
		10	N/A
		01	DIS Board with 4GB VRAM
		00	DIS Board with 2GB VRAM

<Core Design>
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HAD/I2S/SD/DMIC)

Size	Document Number	Rev
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TOUCH PAD/E3

[65,66] PCH_I2C1_SCL_TP
[65,66] PCH_I2C1_SDA_TP

G SENSOR

[70] FFS_INT1

[55,70] SENSOR_I2C_SDA
[55,70] SENSOR_I2C_SCL

[70] GSEN2_INT1_C
[55] GSEN_INT1_C

AUDIO

[27] SPKR

KEYBOARD

[65] KB_LED_BL_DET

OTHER

[24] TABLE_MODE#

[24] NB_MODE#

[91] TPM_SPI_IRQ#

PD

[71] TBT_I2C_SCL
[71] TBT_I2C_SDA

eDP

[55] DBC_PANEL_EN

LID

[24,66] LID_CL_SIO#
[24,66] LID_CL_SIO_TAB#

[68] UART_2_CTXD_DRXD
[68] UART_2_CRXD_DTXD

TOUCH

[55] I2C0_SDA_TS
[55] I2C0_SCL_TS

[55] TOUCH_PANEL_DET#

[55] TOUCH_PANEL_INTR#

[24,64] MASK_SATA_LED#

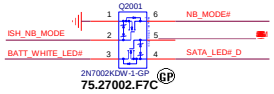
[64] SATA_LED#_D [24,64]

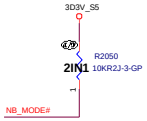
BATT_WHITE_LED#

20200304
KB_LED_BL_DET , GPP_C10 -> GPP_D16
Internal review , follow Nakia
Follow GPIO table

DA51: NRB_BIT
DC49: VGA_DB_DET#
CY49: TPM_PIRQ#
CY53: GC6_THM_DIS#_PCH
CY52: PCH_3.3V_TS_EN
DA50: HDD_FALL_INT
DV21: SBIOS_TX
DR21: USBC0_AUX_N_BIAS
DN21: USBC0_AUX_P_BIAS
DV19: DGPU_MACO_EN
DT19: SIO_EXT_WAKE#
DR18: PCH_HDD_EN
DU19: LCD_CBL_DET#
DG23: cTPM_PRSNT#
DJ19: TOUCH_PANEL_INTR#
DF21: TOUCH_I2C_DET#
DV18: I2C0_SCL_TS
DW18: I2C0_SDA_TS
DF29: DBC_PANEL_EN
DG29: LOM_CABLE_DETECT#
DF25: CNV_COEX1
DF27: CNV_COEX2
DR27: STYLUS_PWR_OCP#
DW27: CAM_SHUTTER#
DY25: IO_DB_DET#
CY39: ISH_I2C1_ALS_SCL
DB47: ISH_I2C1_ALS_SDA
DD47: ISH_I2C2_SCL
DD44: ISH_I2C2_SDA
DJ8: ISH_P_SENSOR_INT#
DV31: ISH_ALS_INT#

DG17: SPCDD_PWR_EN#
DG19: SPCDD_DA#





	NB_MODE	LID_CL_SIO_TAB#	
NB Mode	1	1	KB可以動
Tablet Mode	don´t care	0	KB鎖住
Clam Shell Mode	0	1	KB鎖住

<Core Design>

Wistron Corporation
21F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)

Size	Document Number	Rev
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Main Func = PCH

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<Core Desiign>

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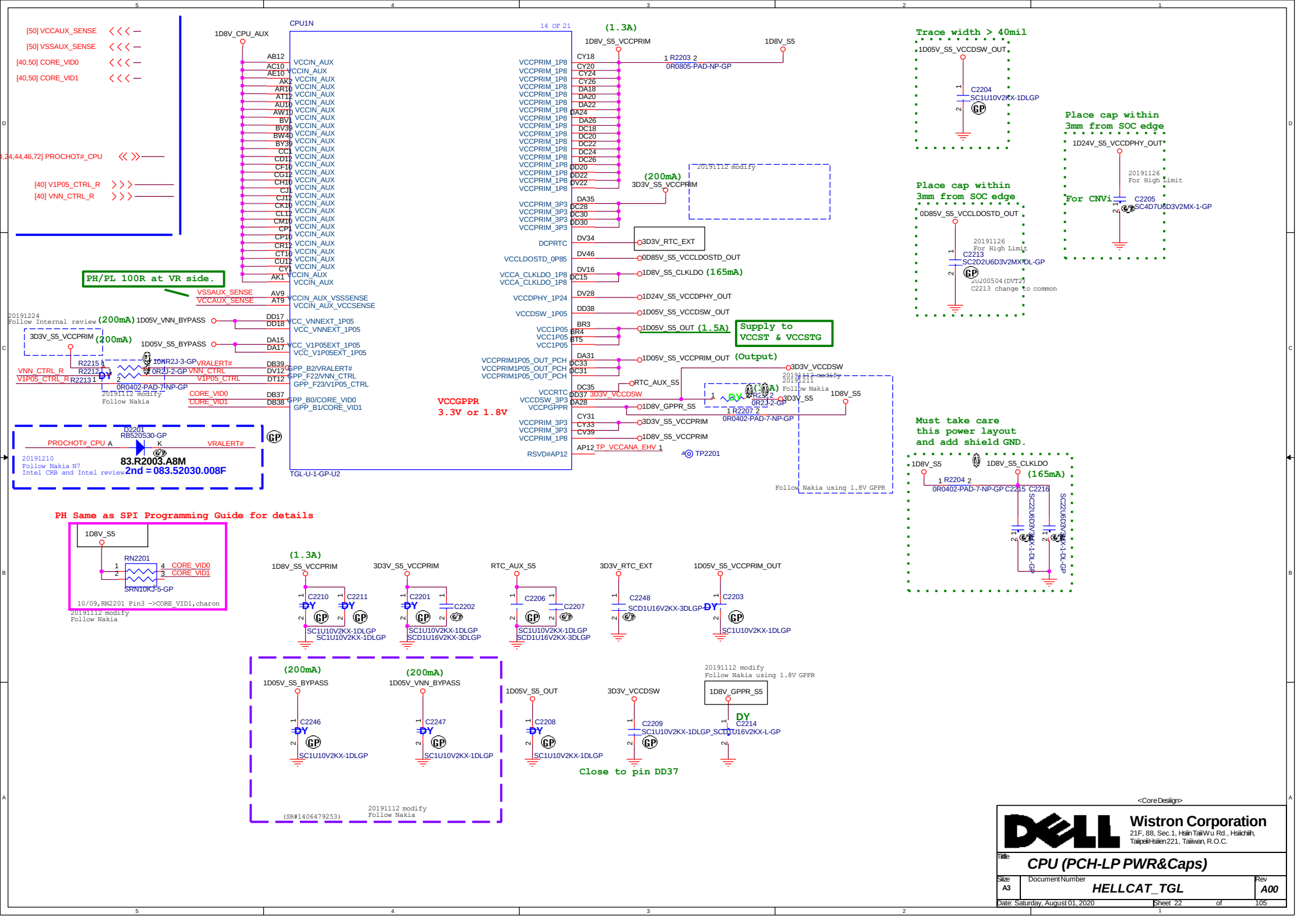
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (CSI/EMMC/CNVi)**

Size	Document Number	Rev
A3	HELLCAT_TGL	A00

Date: Saturday, August 01, 2020 Sheet 21 of 105


CPU1N
14 OF 21
TGL-U-1-GP-U2
[50] VCCAUX_SENSE
[50] VSSAUX_SENSE
[40,50] CORE_VID0
[40,50] CORE_VID1
[40] V1P05_CTRL_R
[40] VNN_CTRL_R
1D8V_CPU_AUX
PH/PL 100R at VR side.
VSSAUX_SENSE
VCCAUX_SENSE
20191224
Follow Internal review
(200mA) 1D05V_VNN_BYPASS
3D3V_S5_VCCPRIM (200mA)
1D05V_S5_BYPASS
VNN_CTRL_R
V1P05_CTRL_R
VRALERT#
VNN_CTRL
V1P05_CTRL
CORE_VID0
CORE_VID1
20191112 modify
Follow Nakia
PROCHOT#_CPU
VRALERT#
D2201
RB520S30-GP
83.R2003.A8M
2nd = 083.52030.008F
20191210
Follow Nakia N7
Intel CRB and Intel review
VCCGPPR
3.3V or 1.8V
(1.3A)
1D8V_S5_VCCPRIM
1D8V_S5
R2203
0R0805-PAD-NP-GP
(200mA)
3D3V_S5_VCCPRIM
20191112 modify
3D3V_RTC_EXT
0D85V_S5_VCCLDOSTD_OUT
1D8V_S5_CLKLDO (165mA)
1D24V_S5_VCCDPHY_OUT
1D05V_S5_VCCDSW_OUT
1D05V_S5_OUT (1.5A)
Supply to
VCCST & VCCSTG
1D05V_S5_VCCPRIM_OUT (Output)
3D3V_VCCDSW
RTC_AUX_S5
1D8V_GPPR_S5
3D3V_S5_VCCPRIM
1D8V_S5_VCCPRIM
TP_VCCANA_EHV
TP2201
20191112 modify
20190211
Follow Nakia
R2207
0R0402-PAD-7-NP-GP
Follow Nakia using 1.8V GPPR
Trace width > 40mil
1D05V_S5_VCCDSW_OUT
C2204
SC1U10V2KX-1DLGP
Place cap within
3mm from SOC edge
0D85V_S5_VCCLDOSTD_OUT
20191126
For High Limit
C2213
SC2D2U6D3V2MX-DL-GP
20200504 (DVT2)
C2213 change to common
Place cap within
3mm from SOC edge
1D24V_S5_VCCDPHY_OUT
20191126
For High Limit
For CNVi
C2205
SC4D7U6D3V2MX-1-GP
Must take care
this power layout
and add shield GND.
1D8V_S5
1D8V_S5_CLKLDO
(165mA)
R2204
0R0402-PAD-7-NP-GP
C2215
C2216
SC22U6D3V2MX-1-DL-GP
PH Same as SPI Programming Guide for details
1D8V_S5
RN2201
CORE_VID0
CORE_VID1
SRN10KJ-5-GP
10/09,RN2201 Pin3 ->CORE_VID1,charon
20191112 modify
Follow Nakia
(1.3A)
1D8V_S5_VCCPRIM
C2210
C2211
SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP
3D3V_S5_VCCPRIM
C2201
C2202
SC1U10V2KX-1DLGP
SCD1U16V2KX-3DLGP
RTC_AUX_S5
C2206
C2207
SC1U10V2KX-1DLGP
SCD1U16V2KX-3DLGP
3D3V_RTC_EXT
C2248
SCD1U16V2KX-3DLGP
1D05V_S5_VCCPRIM_OUT
C2203
SC1U10V2KX-1DLGP
(200mA)
1D05V_S5_BYPASS
C2246
SC1U10V2KX-1DLGP
(200mA)
1D05V_VNN_BYPASS
C2247
SC1U10V2KX-1DLGP
(SR#1406479253)
20191112 modify
Follow Nakia
1D05V_S5_OUT
C2208
SC1U10V2KX-1DLGP
3D3V_VCCDSW
C2209
SC1U10V2KX-1DLGP
Close to pin DD37
20191112 modify
Follow Nakia using 1.8V GPPR
1D8V_GPPR_S5
C2214
SCD1U16V2KX-L-GP
<Core Desiign>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (PCH-LP PWR&Caps)
Size
A3
Document Number
HELLCAT_TGL
Rev
A00
Date: Saturday, August 01, 2020
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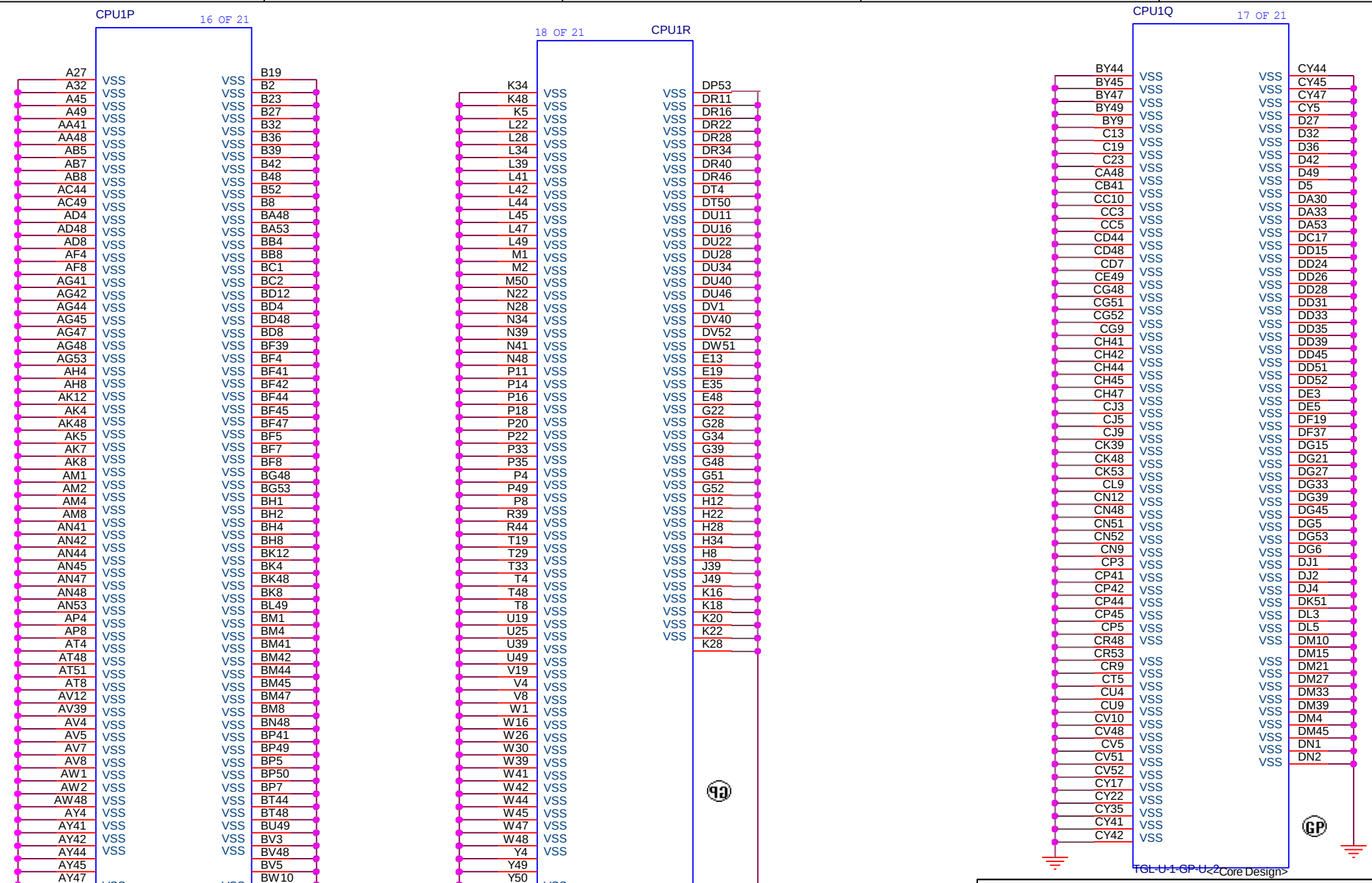


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A4	***HELLCAT_TGL***	***A00***

Date: Saturday, August 01, 2020 | Sheet 23 of 105

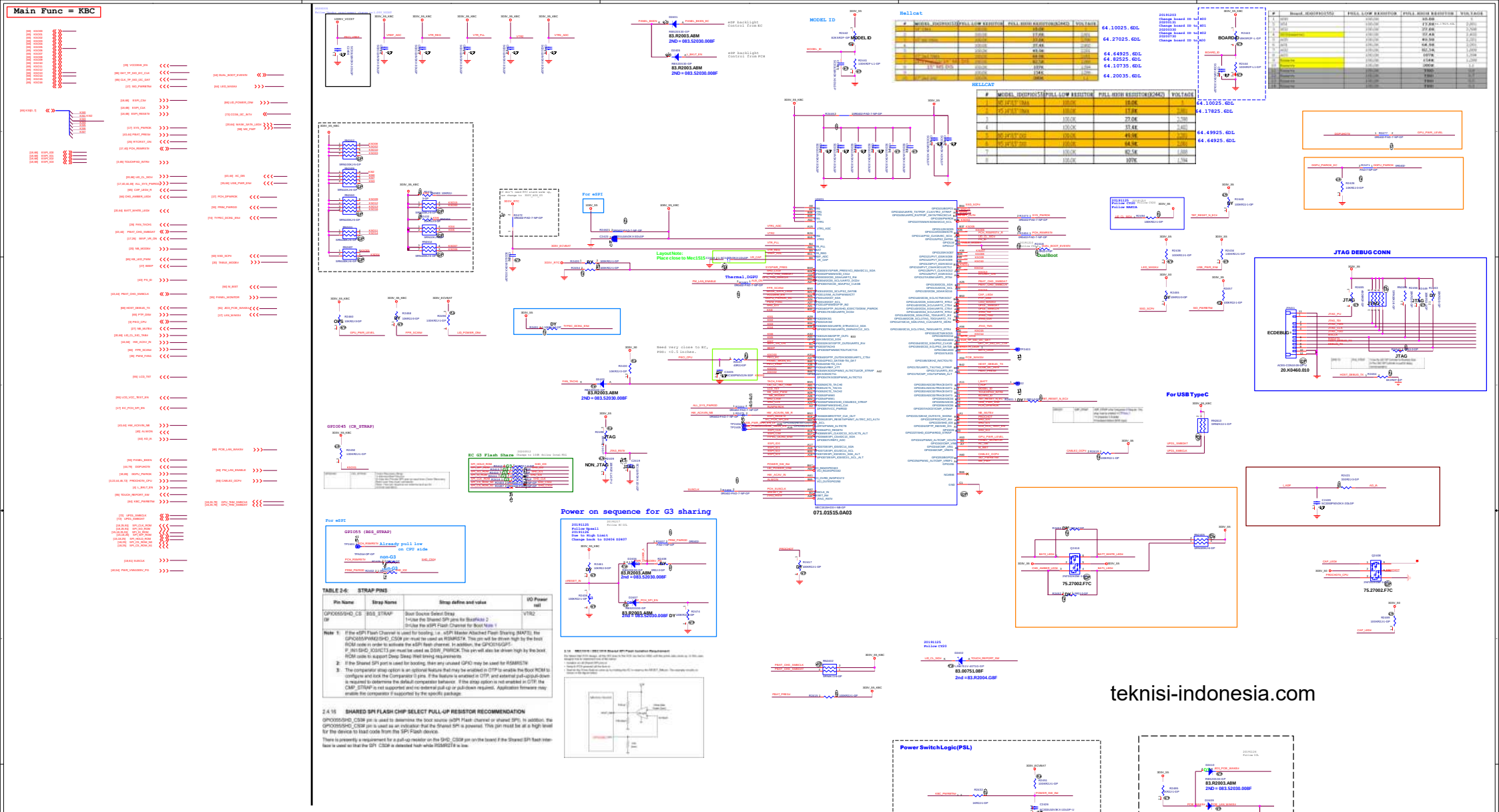


TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO055/SHD_CS0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for BootNode 2 0=Use the eSPI Flash Channel for Boot Node 1	VTR2

Note 1: If the eSPI Flash Channel is used for booting, i.e. eSPI Master Attached Flash Sharing (MAFS), the GPIO055/PWM2/SHD_CS0# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. In addition, the GPIO016/GPT-P_IN1/SHD_IO3/ECT3 pin must be used as DSW_PWROK. This pin will also be driven high by the boot ROM code to support Deep Sleep Well timing requirements

2: If the Shared SPI port is used for booting, then any unused GPIO may be used for RSMRST#

3: The comparator strap option is an optional feature that may be enabled in OTP to enable the Boot ROM to configure and lock the Comparator 0 pins. If the feature is enabled in OTP, and external pull-up/pull-down is required to determine the default comparator behavior. If the strap option is not enabled in OTP, the CMP_STRAP is not supported and no external pull-up or pull-down required. Application firmware may enable the comparator if supported by the specific package.

2.4.16 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/SHD_CS0# pin is used to determine the boot source (eSPI Flash channel or shared SPI). In addition, the GPIO055/SHD_CS0# pin is used as an indicator that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD_CS0# pin on the board if the Shared SPI flash interface is used so that the SPI_CS0# is detected high while RSMRST# is low.

DELL Wiistron Corporatiiion

KBC NuvotonNPCE285PA0DX

MOCKIIINGBIIIRD_TGL

A00

Main Func = SPI Flash

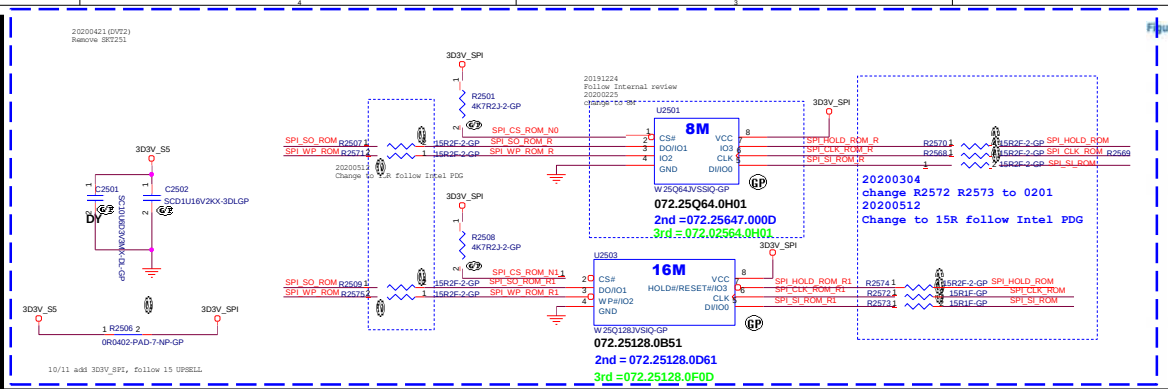
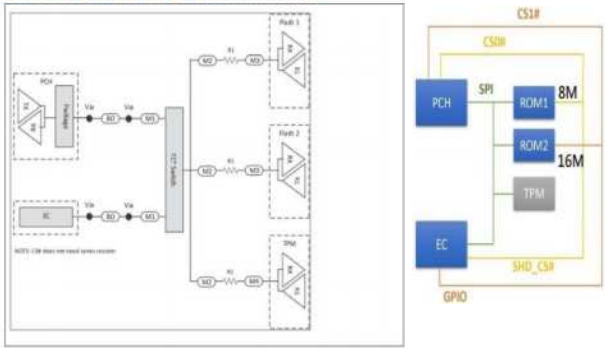
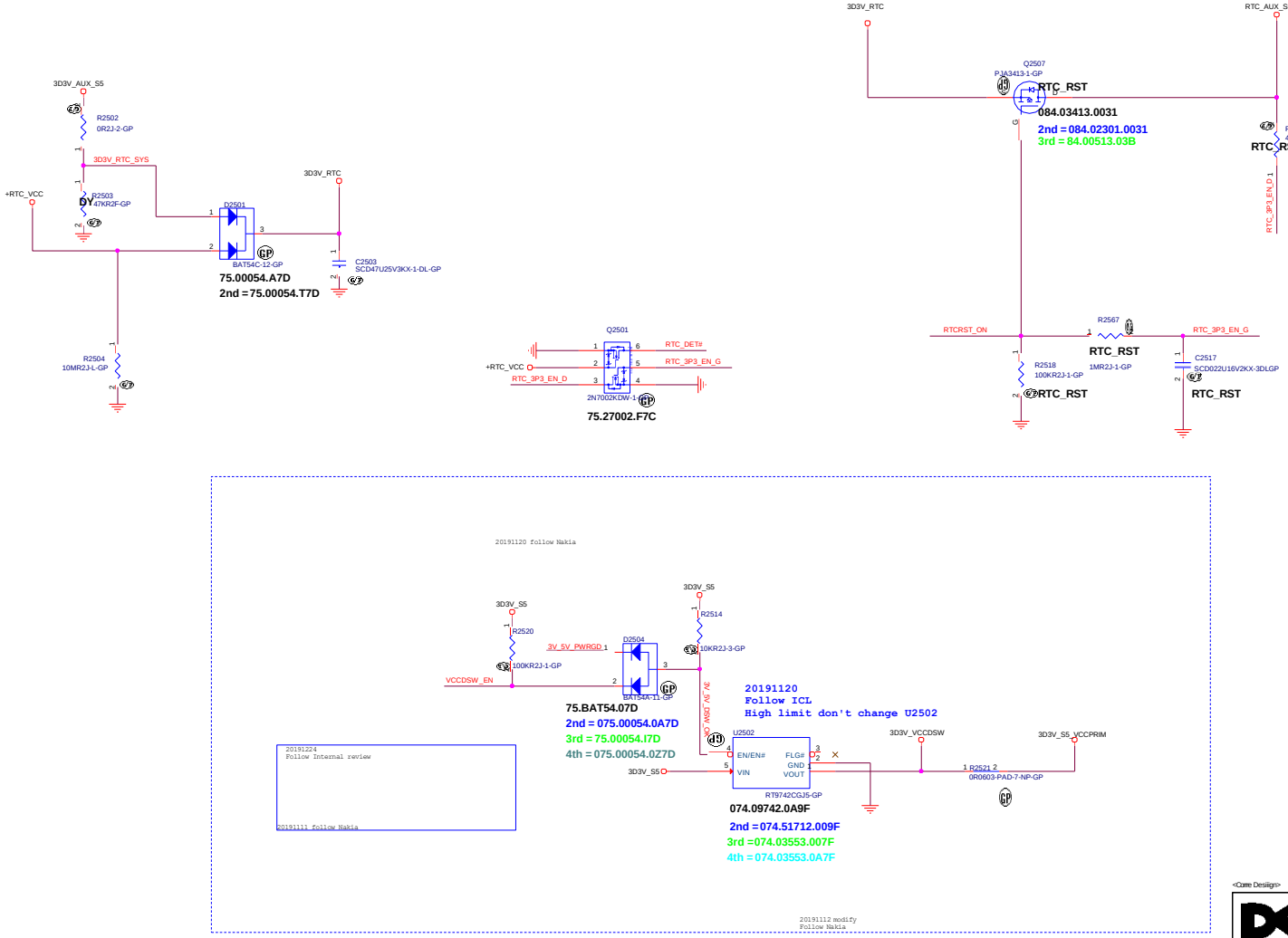


Figure 217. SPI0 3-Load EC G3 Flash Sharing with FET Isolation Topology



Main Func = RTC



<Core Desiign>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash

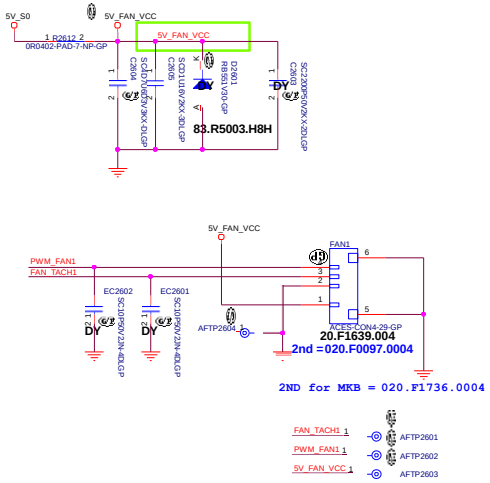
Size	Document Number	Rev
A2	HELLCAT_TGL	A00

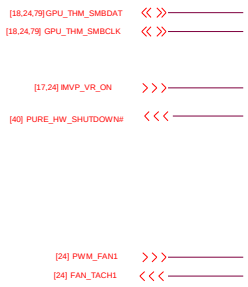
Date: Saturday, August 01, 2020 Sheet 25 of 105

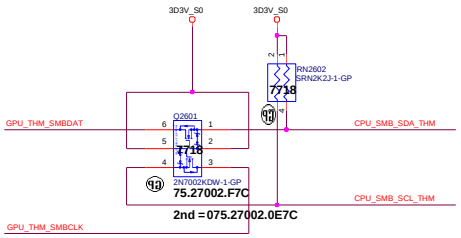
Main Func = Thermal Sensor

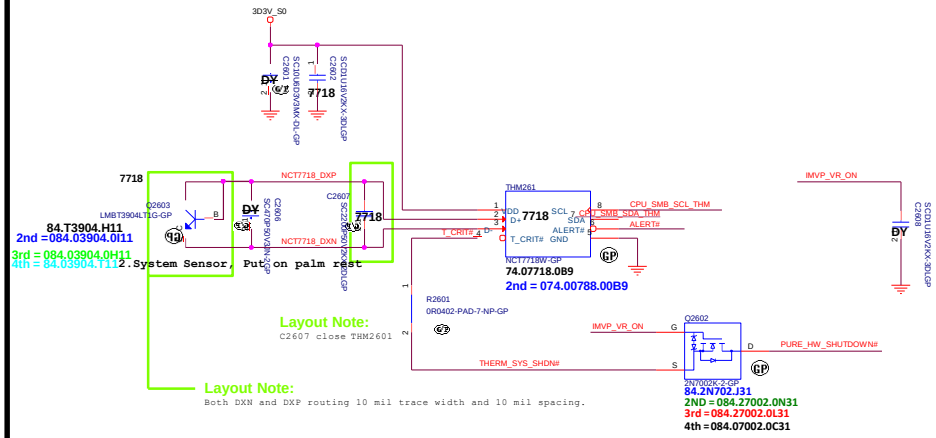
PWM FAN1

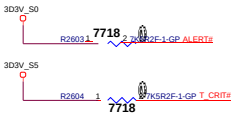
Layout Note:
Signal Routing Guideline:
Trace width = 15mil











TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

<Core Design>
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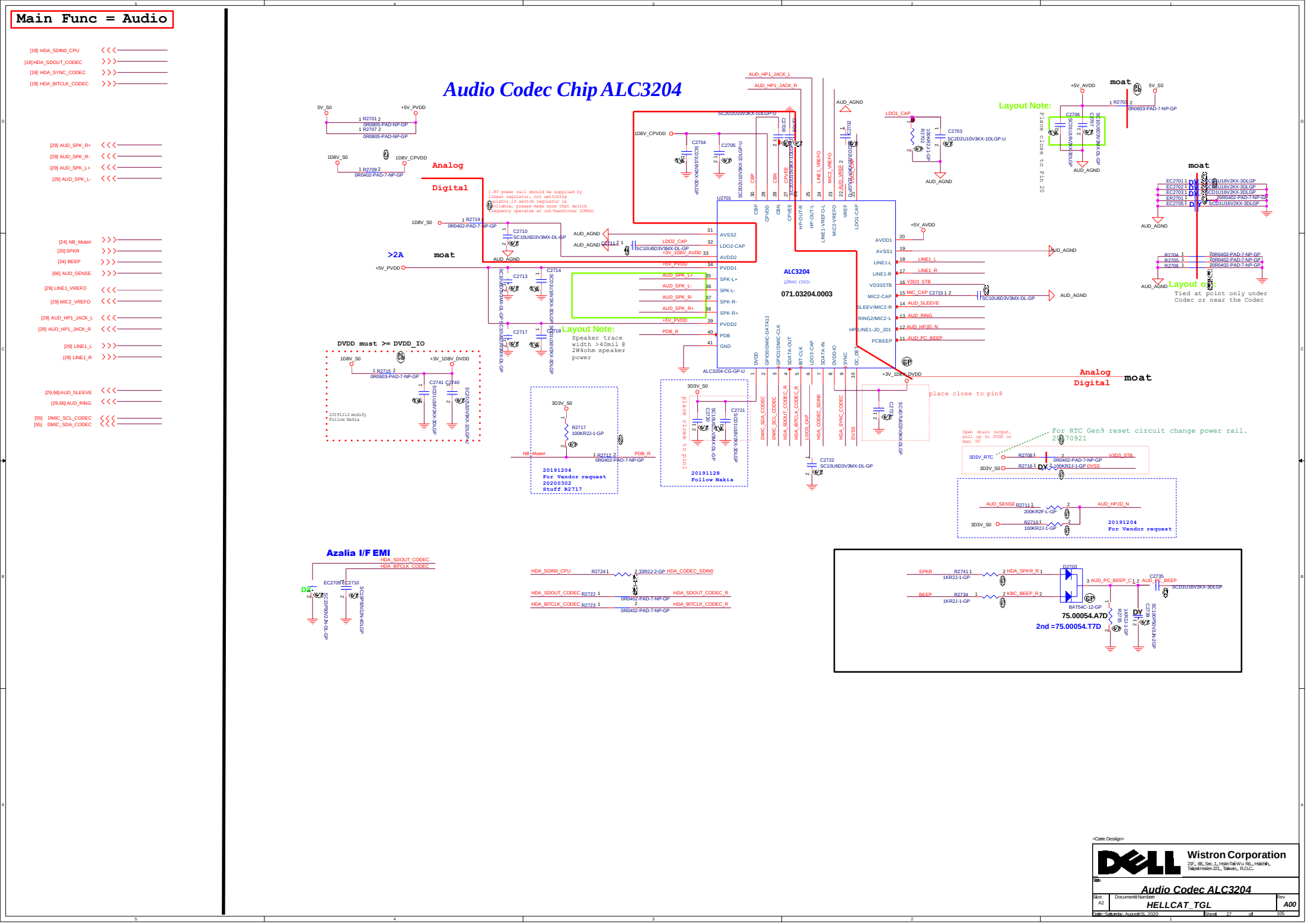
Title: THERMAL NCT7718W/Fan
Size A2 | Document Number: HELLCAT_TGL | Rev A00
Date: Saturday, August 01, 2020 | Sheet 26 of 105



<Core Design>

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Title: Audio Codec ALC3204

Size	Document Number	Rev
A2	HELLCAT_TGL	A00

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Main Func = Audio

[27] AUD_SPK_R+
[27] AUD_SPK_R-
[27] AUD_SPK_L-
[27] AUD_SPK_L+

[18] SPK_ID

Speaker

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

AUD_SPK_L+ R29021 2 0R0603-PAD-7-NP-GP
AUD_SPK_L- R29011 2 0R0603-PAD-7-NP-GP
AUD_SPK_R- R29031 2 0R0603-PAD-7-NP-GP
AUD_SPK_R+ R29041 2 0R0603-PAD-7-NP-GP

SPK1 — MKB — ACES-CON6-20-GP-U
20.F1639.006
2nd = 020.F1263.0006

SPK2 — Hellcat — ACES-CON4-29-GP
20.F1639.004
2nd = 020.F0097.0004

ED2901 ED2902 ED2903 ED2904 ED2905 — AZ5725-01FDR7G-GP
83.05725.0A0 83.05725.0A0 83.05725.0A0
83.05725.0A0 83.05725.0A0

EC2902 EC2901 EC2903 EC2904 — SC1KF50V2KX-1DLGP

CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

SPK_ID 1: VECO
0: ZY

AFTP2901 AFTP2902 AFTP2903 AFTP2904 AFTP2911

From Codec

[27] MIC2_VREFO
[27,29,66] AUD_RING
[27] AUD_HP1_JACK_L
[27] LINE1_L
[27] LINE1_R
[27] AUD_HP1_JACK_R
[27,29,66] AUD_SLEEVE
[27] LINE1_VREFO

Universal Jack (Moved to I/O Board)

RN2901 SRN2K2J-1-GP
MIC2_VREFO
AUD_HP1_JACK_L — LINE1_L_C2907 — LINE1-L_C R29221 1KR2J-1-GP — SC10U6D3V3MX-DL-GP — R29081 10R2F-L-GP — AUD_RING / AUD_HP1_JACK_L1
LINE1_R_C2908 — LINE1-L_R R29211 1KR2J-1-GP — SC10U6D3V3MX-DL-GP — R29101 10R2F-L-GP — AUD_HP1_JACK_R / AUD_SLEEVE
AUD_HP1_JACK_R

LINE1_VREFO — D2901 RB520S30-GP — LINE1_VREFO_D1 R2912 4K7R2J-2-GP
83.R2003.A8M
2ND = 083.52030.008F
D2902 RB520S30-GP — LINE1_VREFO_D2 R2913 4K7R2J-2-GP
83.R2003.A8M
2ND = 083.52030.008F

To IO Board

[27,29,66] AUD_RING
[66] AUD_HP1_JACK_L1
[66] AUD_HP1_JACK_R1
[27,29,66] AUD_SLEEVE

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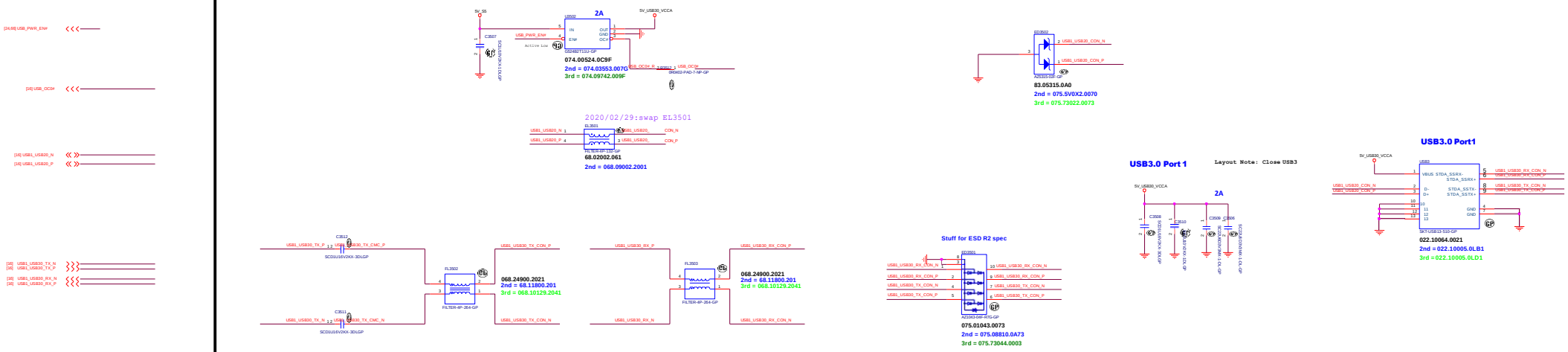
Title: Audio IO
Size: A3 | Document Number: HELLCAT_TGL | Rev: A00
Date: Saturday, August 01, 2020 | Sheet 29 of 105

Main Func = USB3.0 Port1



<Core Design>

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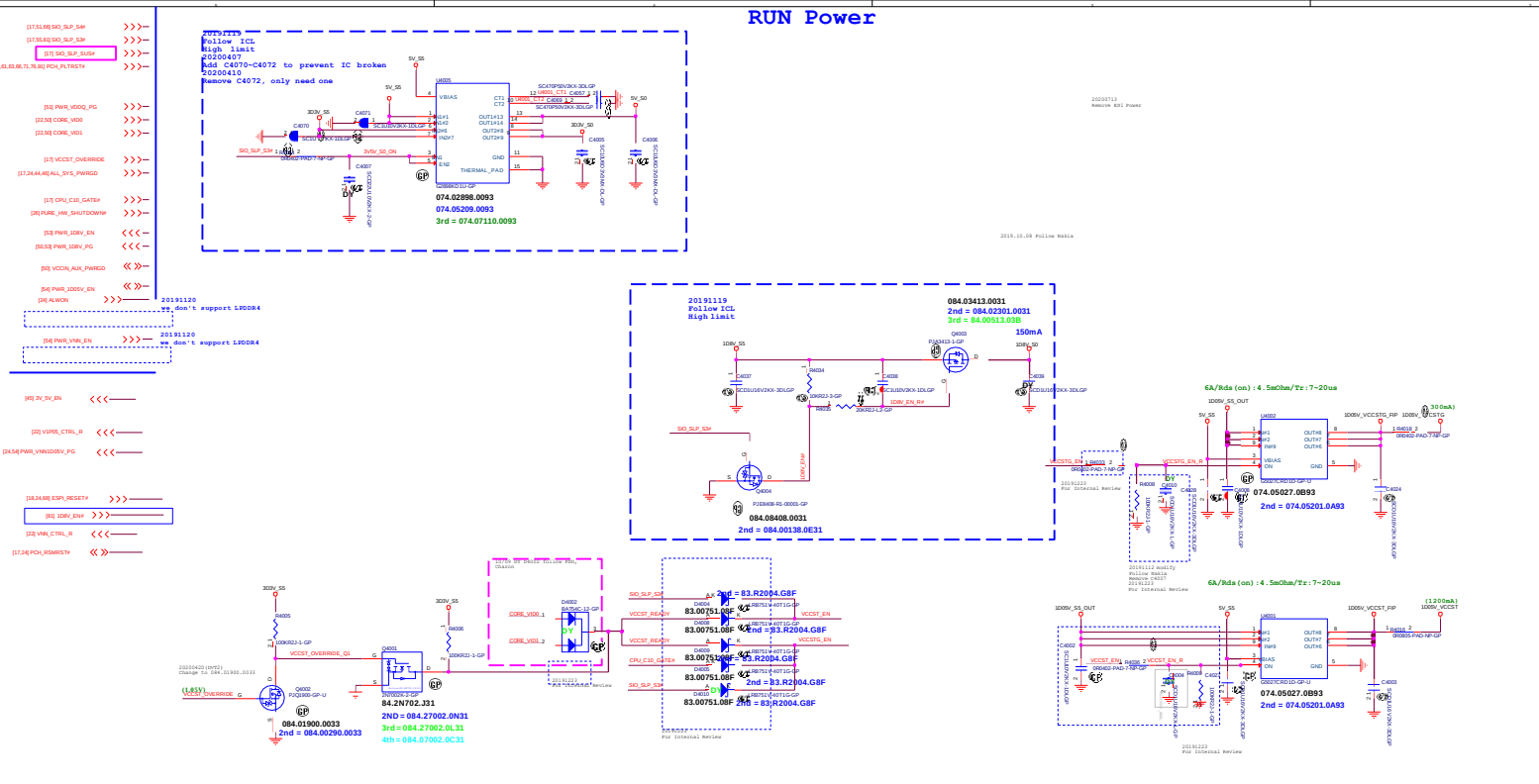
Title: USB3.0CONN

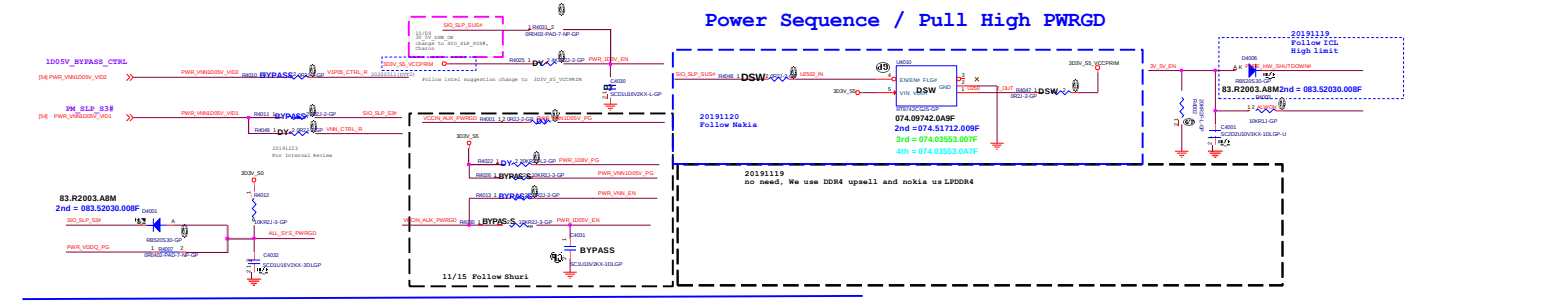
Size	Document Number	Rev
A1	HELLCAT_TGL	A00

Date: Saturday, August 01, 2020 Sheet 25 of 105

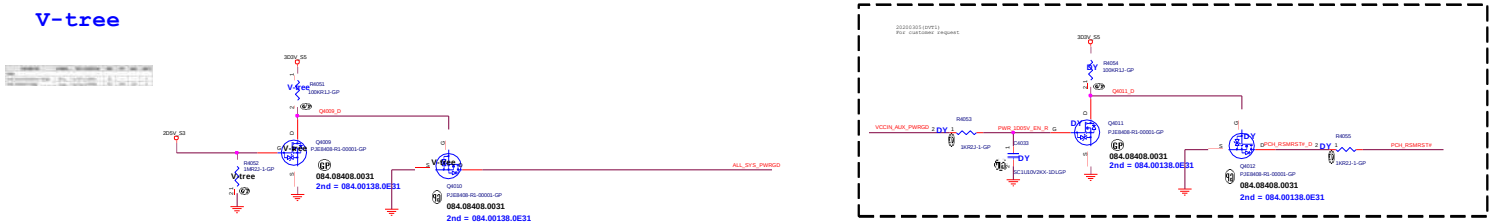
RUN Power



Power Sequence / Pull High PWRGD



V-tree



Wistron Corporation

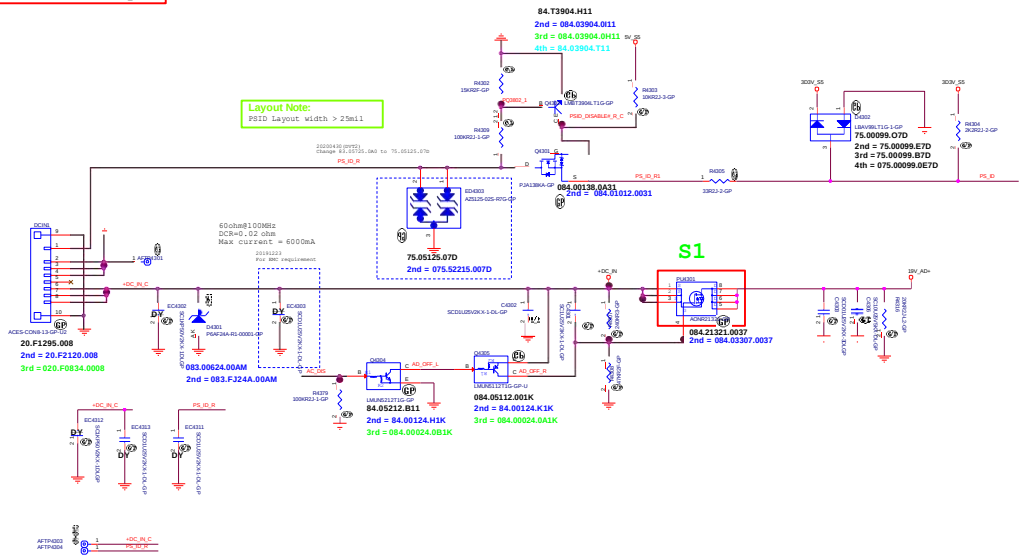
CPU(THML/JTAG)

HELLCAT_TGL

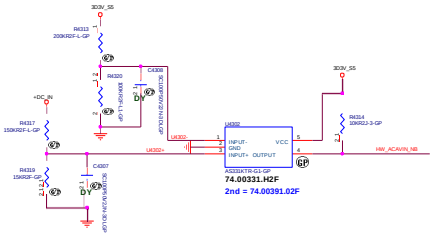
A00

[24,44] AC_DIS
[24] PS_ID
[24,44] HW_ACAVIN_NB
[44,88] +DC_IN_C
[44,88] +DC_IN

Main Func = ADT Input

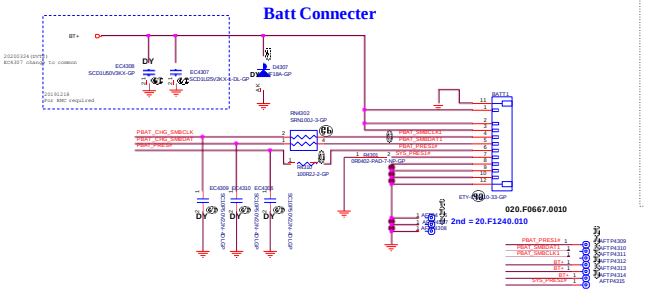


Barrel Adapter Piug-in Detect

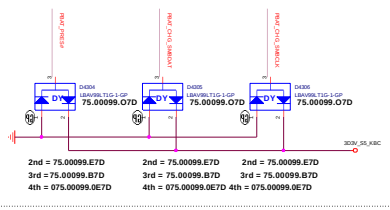


[24,44] PBAT_CHG_SMBCLK
[24,44] PBAT_CHG_SMBDAT
[24,44] PBAT_PRESH

Main Func = M-BAT Input



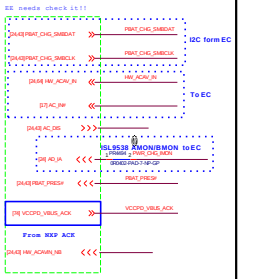
Placement: Close to Batt Connector

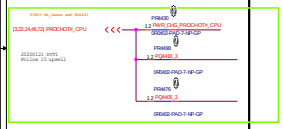


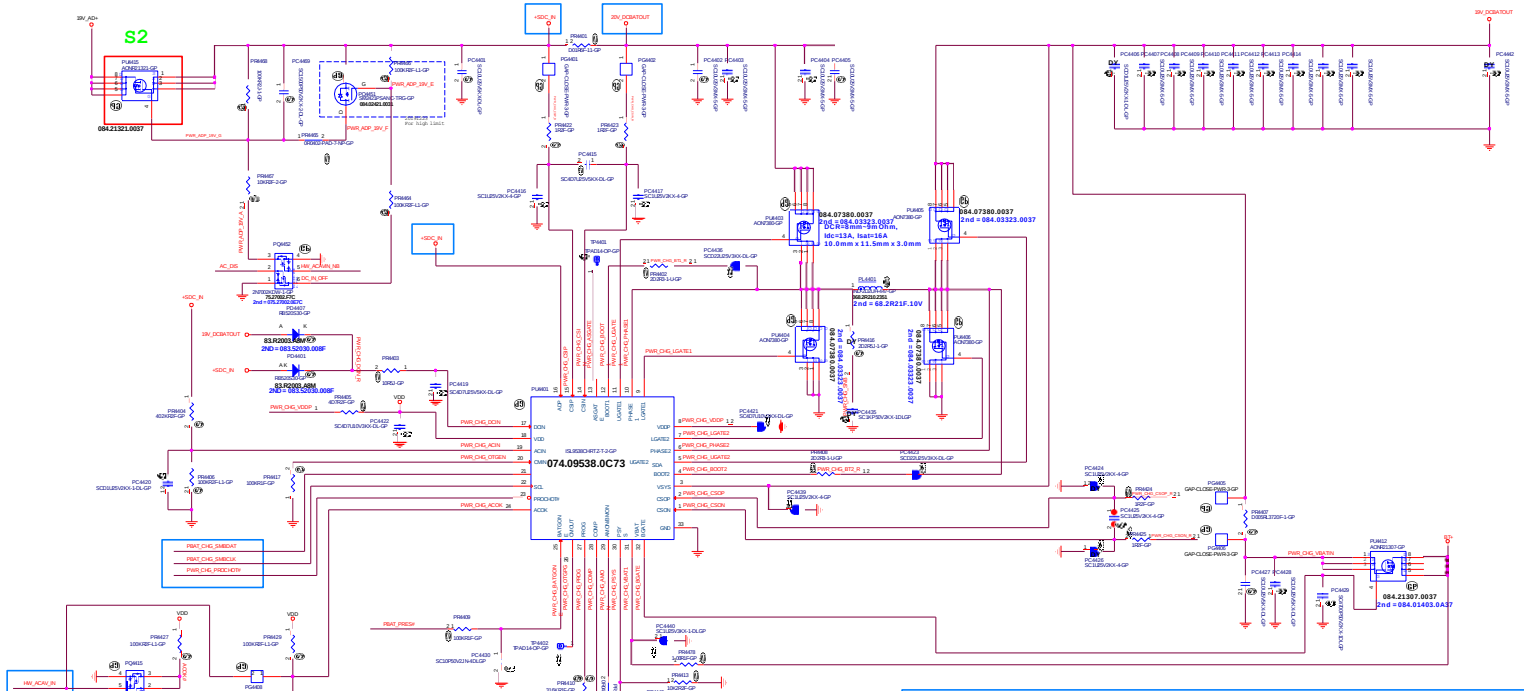
Main Func = Charger

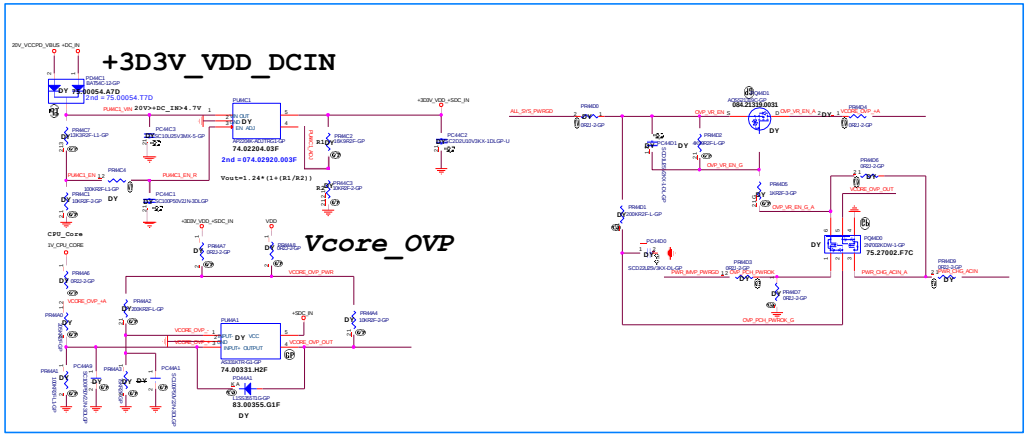
ISL9538C For Charger

OFFPAGE

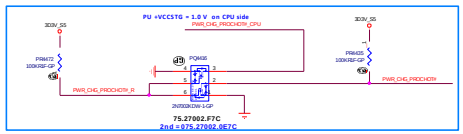


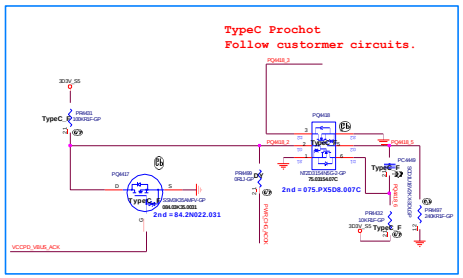






0523





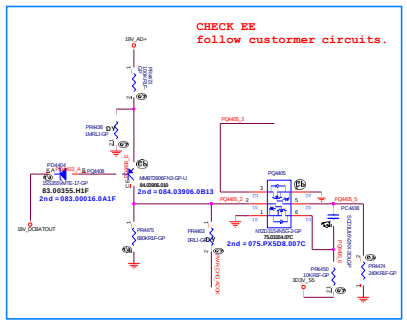


TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ)			CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
MIN	TYP 1%	MAX				
0			1	733kHz	No	0.475
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.475
28.0				733kHz	Yes	0.475
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.475
61.9				1MHz	No	0.475
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.475
105			3	733kHz	No	0.475
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.475
162				733kHz	Yes	0.475
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.475
237				1MHz	No	0.475
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.475
348			1	733kHz	No	0.475

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DATA NEW

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Power (Charger_ISL9538)

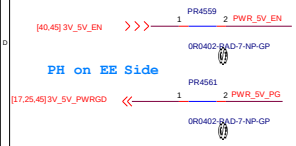
MOCKINGBIRD_TGL

A00

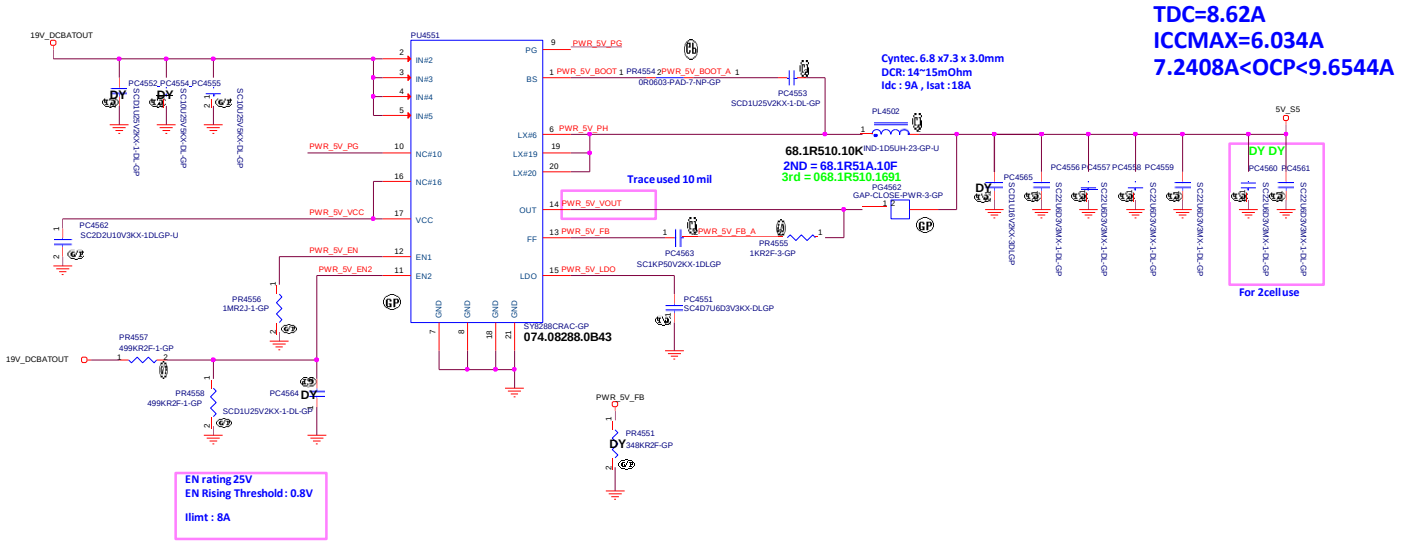
SSID = PWR.Plane.Regulator_5V

OFFPAGE-Signal

OFFPAGE-GAP



SY8288C For 5V

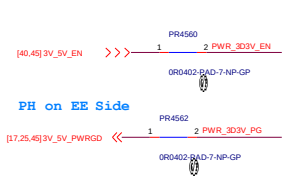


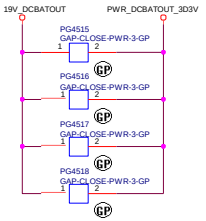
TDC=8.62A
ICCMAX=6.034A
7.2408A<OCP<9.6544A

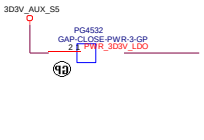
SSID = PWR.Plane.Regulator_3D3V

OFFPAGE-Signal

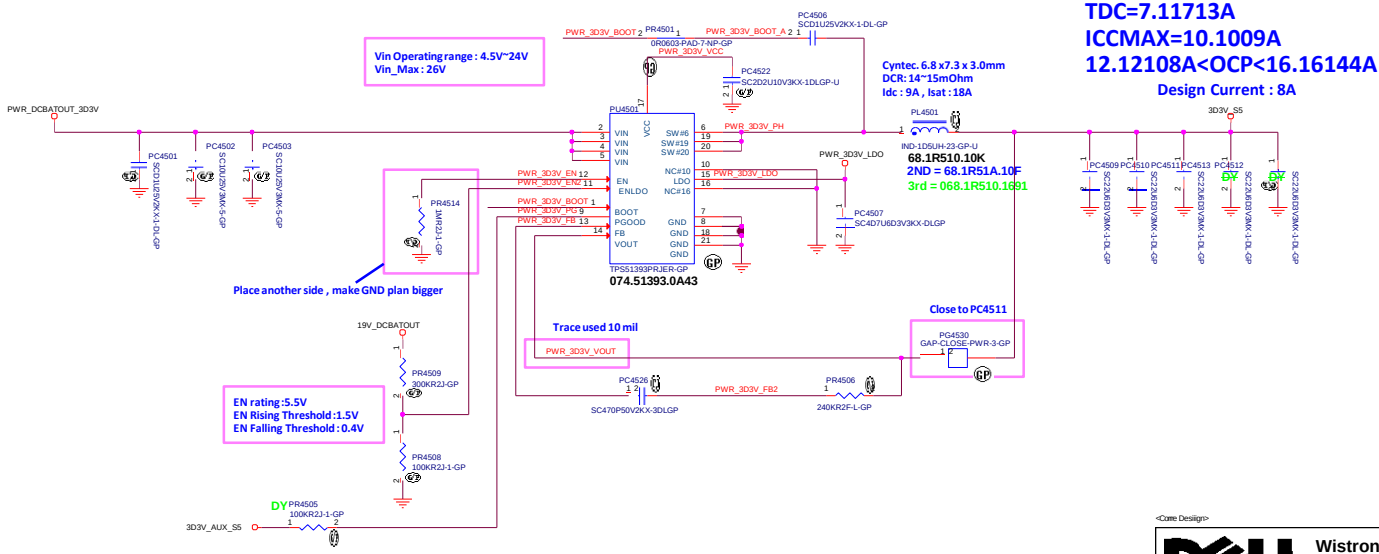
OFFPAGE-GAP







TPS51393 For 3D3V



TDC=7.11713A
ICCMAX=10.1009A
12.12108A<OCP<16.16144A
Design Current : 8A

<Core Design>

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Title: POWER (SY8288_5V/3D3V)

Size	Document Number	Rev
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Main Func = CPU_CORE

OFFPAGE

SVID

20200511(DVT2)
Remove PR4632+PR4634 to Keep away PWR_VCORE_SDIO_R to PWR_VGA_NVVDD8_LGATE1 40mil

[7] SVID_CLK_CPU
[7] SVID_DATA_CPU
[7] SVID_ALERT#_CPU

[3,22,24,44,72] PROCHOT#_CPU — PROCHOT#_CPU
[44] CHGR_PSYS_IMVP — CHGR_PSYS_IMVP
20191119
check with Nakia need change netname to PWR_VCORE_VR_READY or not
[17,44] PWR_IMVP_PWRGD — 1 PR4636 2 0R0402-PAD-7-NP-GP — PWR_VCORE_VR_READY
[17,24,40,44] ALL_SYS_PWRGD — ALL_SYS_PWRGD

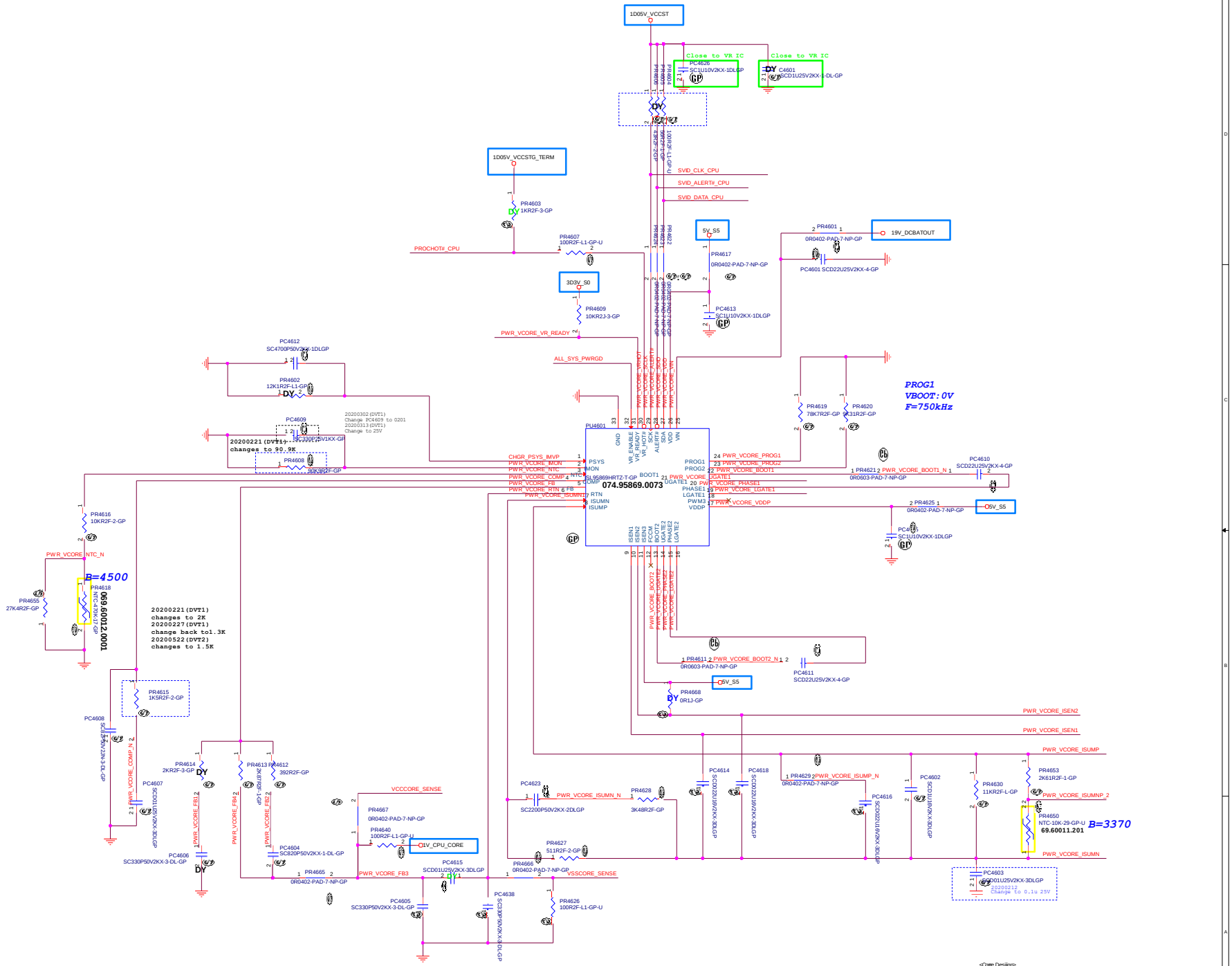
VCORE SENSE

[7] VSSCORE_SENSE — VSSCORE_SENSE
[7] VCCCORE_SENSE — VCCCORE_SENSE

[47] PWR_VCORE_UGATE1 — PWR_VCORE_UGATE1
[47] PWR_VCORE_PHASE1 — PWR_VCORE_PHASE1
[47] PWR_VCORE_LGATE1 — PWR_VCORE_LGATE1

[47] PWR_VCORE_UGATE2 — PWR_VCORE_UGATE2
[47] PWR_VCORE_PHASE2 — PWR_VCORE_PHASE2
[47] PWR_VCORE_LGATE2 — PWR_VCORE_LGATE2

[47] PWR_VCORE_ISEN2 — PWR_VCORE_ISEN2
[47] PWR_VCORE_ISEN1 — PWR_VCORE_ISEN1
[47] PWR_VCORE_ISUMP — PWR_VCORE_ISUMP
[47] PWR_VCORE_ISUMN — PWR_VCORE_ISUMN



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Title: POWER (95869_CPUCORE(1/3))

Size	Document Number	Rev
A2	HELLCAT_TGL	A00

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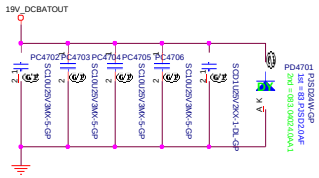
Main Func = VCCIN

OFFPAGE

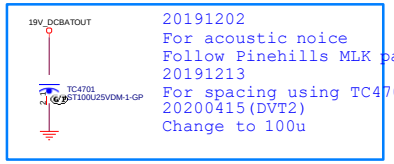
[46] PWR_VCORE_UGATE1 — PWR_VCORE_UGATE1
[46] PWR_VCORE_PHASE1 — PWR_VCORE_PHASE1
[46] PWR_VCORE_LGATE1 — PWR_VCORE_LGATE1

[46] PWR_VCORE_UGATE2 — PWR_VCORE_UGATE2
[46] PWR_VCORE_PHASE2 — PWR_VCORE_PHASE2
[46] PWR_VCORE_LGATE2 — PWR_VCORE_LGATE2

[46] PWR_VCORE_ISEN2 — PWR_VCORE_ISEN2
[46] PWR_VCORE_ISEN1 — PWR_VCORE_ISEN1
[46] PWR_VCORE_ISUMP — PWR_VCORE_ISUMP
[46] PWR_VCORE_ISUMN — PWR_VCORE_ISUMN

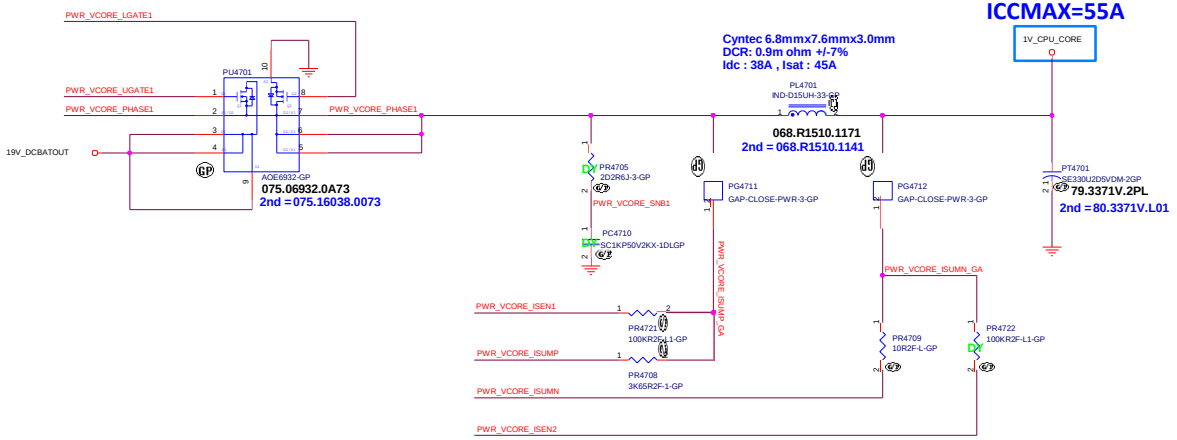


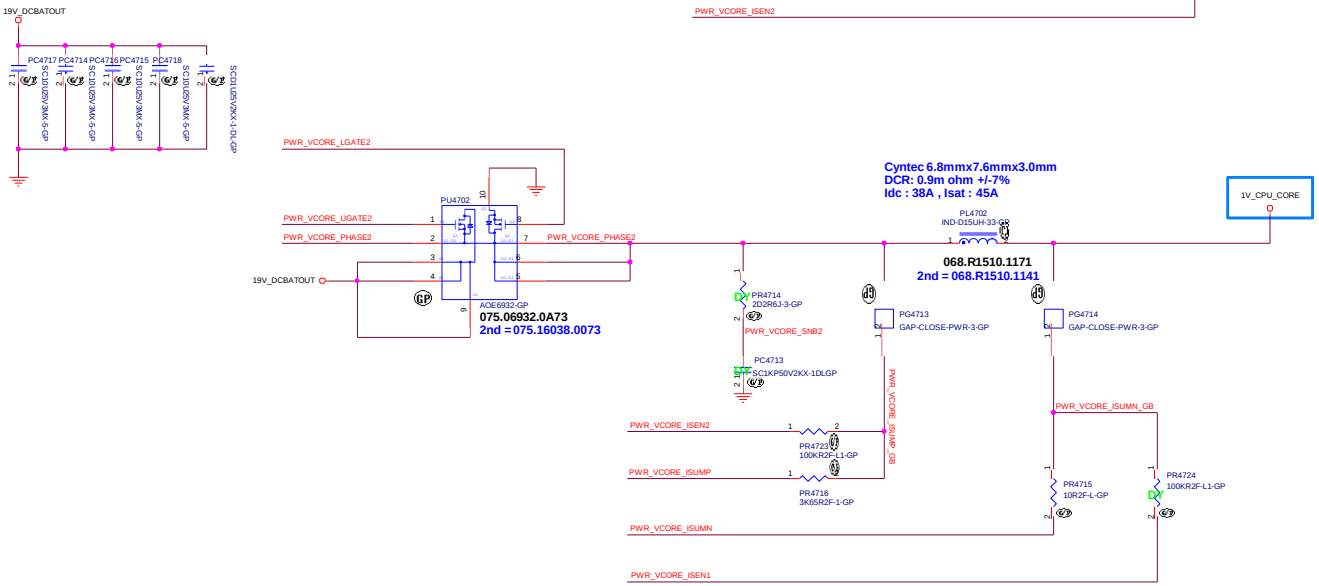
20191202
Change PL4703 PL4704 to R4701 R4702
Follow Pinehills MLK parts
20200508
Change to L4701 L4702
20200728
Change back to R4701 R4702 for Power team request



20191202
For acoustic noice
Follow Pinehills MLK parts
20191213
For spacing using TC4701 only
20200415(DVT2)
Change to 100u

TGL_U42 28W
Baseline
TDC=36A
ICCMAX=55A





<Core Desiign>

Wistron Corporation
21F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (95829_CPUCORE(2/3))

Size	Document Number	Rev
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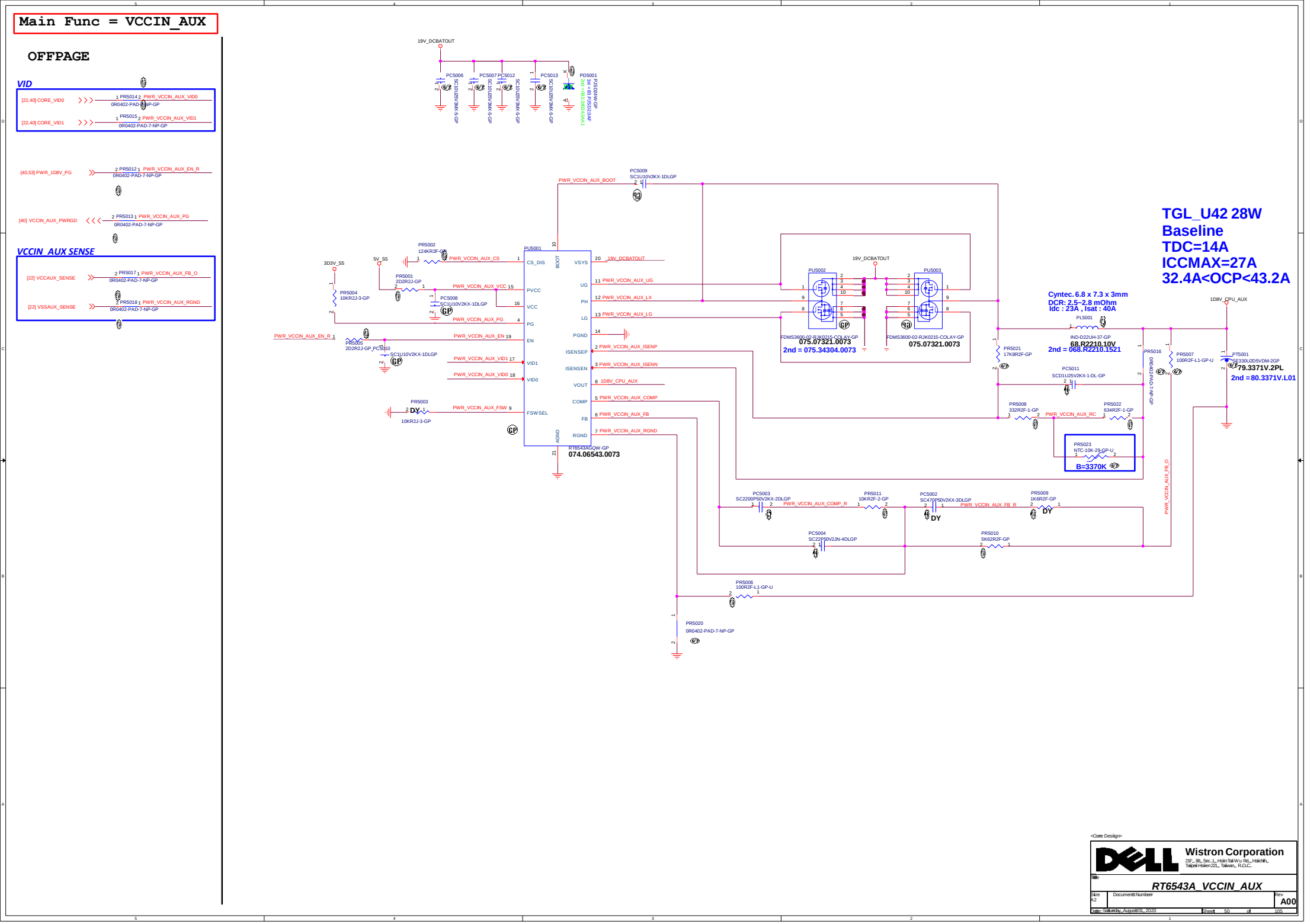
Date: Saturday, August 01, 2020 Sheet 47 of 105



Main Func = VCCIN_AUX
OFFPAGE
VID
[22,40] CORE_VID0
PR5014 PWR_VCCIN_AUX_VID0
0R0402-PAD-7-NP-GP
[22,40] CORE_VID1
PR5015 PWR_VCCIN_AUX_VID1
0R0402-PAD-7-NP-GP
[40,53] PWR_1D8V_PG
PR5012 PWR_VCCIN_AUX_EN_R
0R0402-PAD-7-NP-GP
[40] VCCIN_AUX_PWRGD
PR5013 PWR_VCCIN_AUX_PG
0R0402-PAD-7-NP-GP
VCCIN_AUX SENSE
[22] VCCAUX_SENSE
PR5017 PWR_VCCIN_AUX_FB_O
0R0402-PAD-7-NP-GP
[22] VSSAUX_SENSE
PR5018 PWR_VCCIN_AUX_RGND
0R0402-PAD-7-NP-GP
19V_DCBATOUT
PC5006
PC5007
PC5012
PC5013
PD5001
PJSD2WK-GP
PWR_VCCIN_AUX_BOOT
PC5009
SC1U10V2KX-1DLGP
PU5001
CS_DIS
PVCC
VCC
PG
EN
VID1
VID0
FSWSEL
BOOT
AGND
VSYS
UG
PH
LG
PGND
ISENSEP
ISENSEN
VOUT
COMP
FB
RGND
RT6543AGQW-GP
074.06543.0073
3D3V_S5
5V_S5
PR5002
124KR2F-GP
PWR_VCCIN_AUX_CS
PR5001
2D2R2J-GP
PR5004
10KR2J-3-GP
PWR_VCCIN_AUX_VCC
PC5008
SC1U10V2KX-1DLGP
PWR_VCCIN_AUX_PG
PWR_VCCIN_AUX_EN_R
PR5005
2D2R2J-GP
PC5010
SC1U10V2KX-1DLGP
PWR_VCCIN_AUX_EN
PWR_VCCIN_AUX_VID1
PWR_VCCIN_AUX_VID0
PR5003
DY
10KR2J-3-GP
PWR_VCCIN_AUX_FSW
19V_DCBATOUT
PWR_VCCIN_AUX_UG
PWR_VCCIN_AUX_LX
PWR_VCCIN_AUX_LG
PWR_VCCIN_AUX_ISENP
PWR_VCCIN_AUX_ISENN
1D8V_CPU_AUX
PWR_VCCIN_AUX_COMP
PWR_VCCIN_AUX_FB
PWR_VCCIN_AUX_RGND
PU5002
PU5003
FDMS3600-02-RJK0215-COLAY-GP
075.07321.0073
2nd = 075.34304.0073
075.07321.0073
TGL_U42 28W
Baseline
TDC=14A
ICCMAX=27A
32.4A<OCP<43.2A
Cyntec. 6.8 x 7.3 x 3mm
DCR: 2.5~2.8 mOhm
Idc : 23A , Isat : 40A
PL5001
IND-D22UH-37-GP
68.R2210.10V
2nd = 068.R2210.1521
PR5021
17K8R2F-GP
PC5011
SCD1U25V2KX-1-DL-GP
PR5016
0R0402-PAD-7-NP-GP
PR5007
100R2F-L1-GP-U
1D8V_CPU_AUX
PT5001
SE330U2D5VDM-2GP
79.3371V.2PL
2nd = 80.3371V.L01
PR5008
332R2F-1-GP
PWR_VCCIN_AUX_RC
PR5022
634R2F-1-GP
PR5023
NTC-10K-29-GP-U
B=3370K
PWR_VCCIN_AUX_FB_O
PC5003
SC2200P50V2KX-2DLGP
PWR_VCCIN_AUX_COMP_R
PR5011
10KR2F-2-GP
PC5002
SC470P50V2KX-3DLGP
PWR_VCCIN_AUX_FB_R
PR5009
1K6R2F-GP
DY
PC5004
SC22P50V2JN-4DLGP
PR5010
5K62R2F-GP
PR5006
100R2F-L1-GP-U
PR5020
0R0402-PAD-7-NP-GP
<Core Design>
Wistron Corporation
21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RT6543A_VCCIN_AUX
Size
A2
Document Number
Rev
A00
Date: Saturday, August 01, 2020
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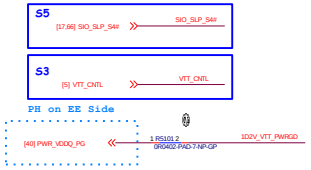
OFFPAGE



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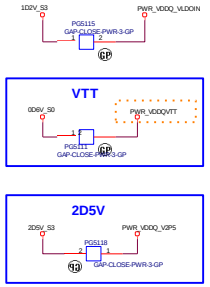

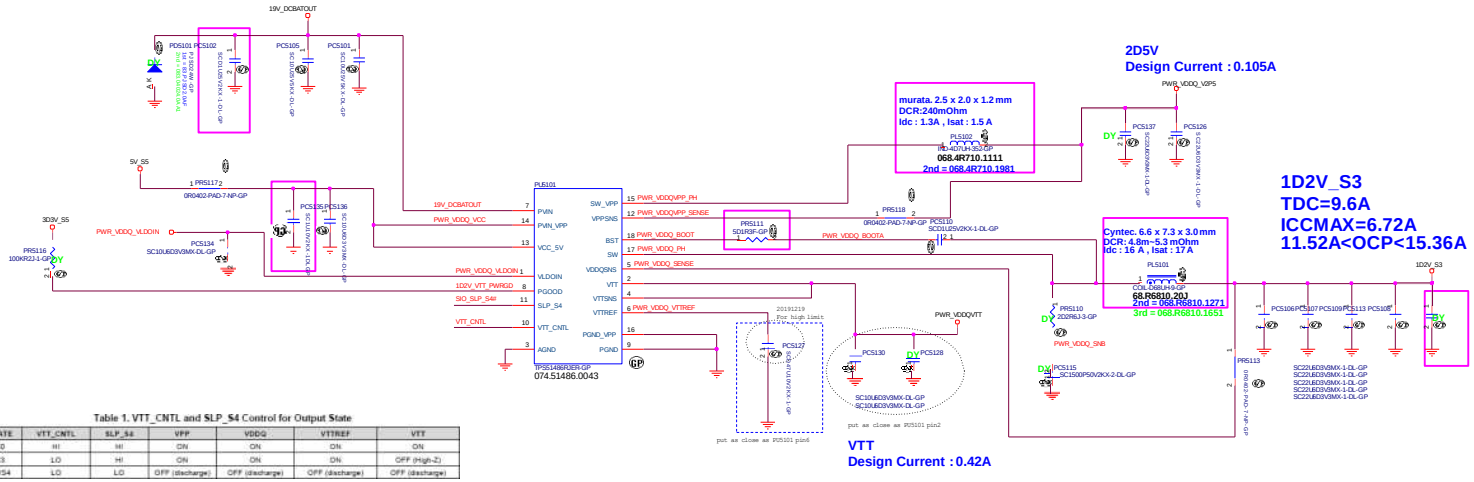

Table 1. VTT_CNTL and SLP_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

<Core Design>

Wistron Corporation
2F., 88, Sec. 1, Hsin Tai Wu Rd., Hsi Chih,
Taipei Hsien 221, Taiwan, R.O.C.

051_POWER (TPS51486R_VDDQ/VTT)

Size	Document Number	Rev
Custom	HELLCAT_TGL	A00

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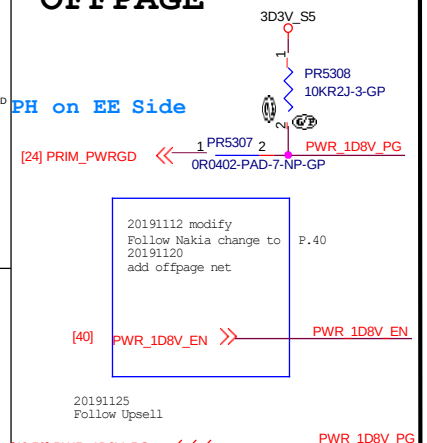
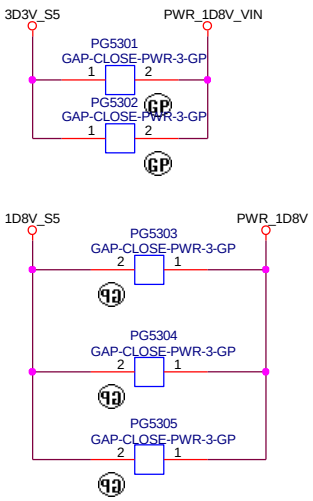
Main Func = 1D8V/1D2V

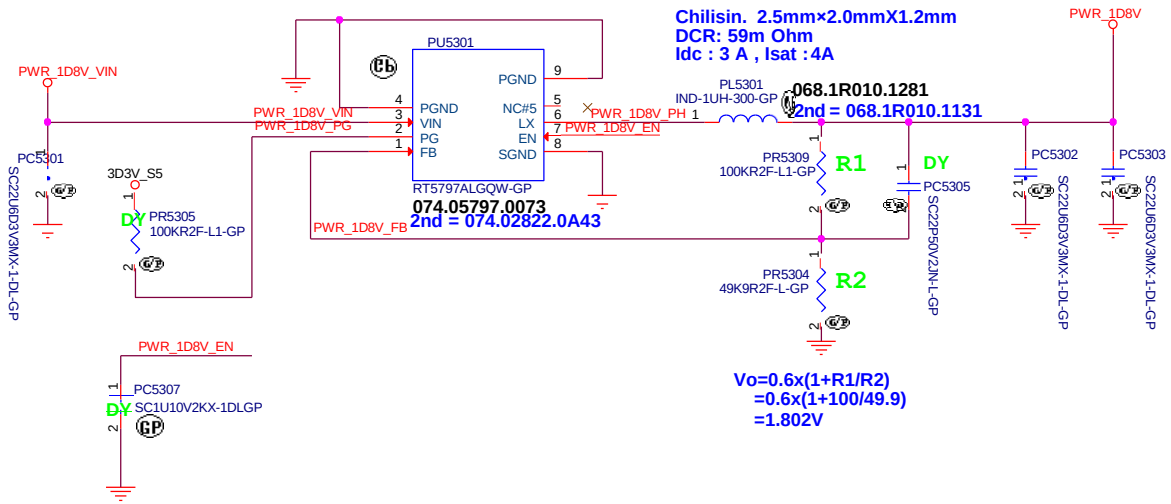
OFFPAGE



OFFPAGE_GAP



TDC=1.029A
ICCMAX=1.47A
1.764A<OCP<2.352A



Vo=0.6x(1+R1/R2)
=0.6x(1+100/49.9)
=1.802V

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	*LCD&CAM&DMC&Touch*	
Size B	Document Number HELLCAT_TGL	Rev A00
Date: Saturday, August 01, 2020	Sheet 53 of 105	

Main Func = 1D05V

OFFPAGE

PH on EE Side

20191119
Check with UPSELL and Nakia follow which one

VCCIN_AUX_PWRGD
[40] PWR_VNN_EN — PWR_VNN_EN

1D05V_BP_PWRGD
[24,40] PWR_VNN1D05V_PG — PWR_VNN1D05V_PG

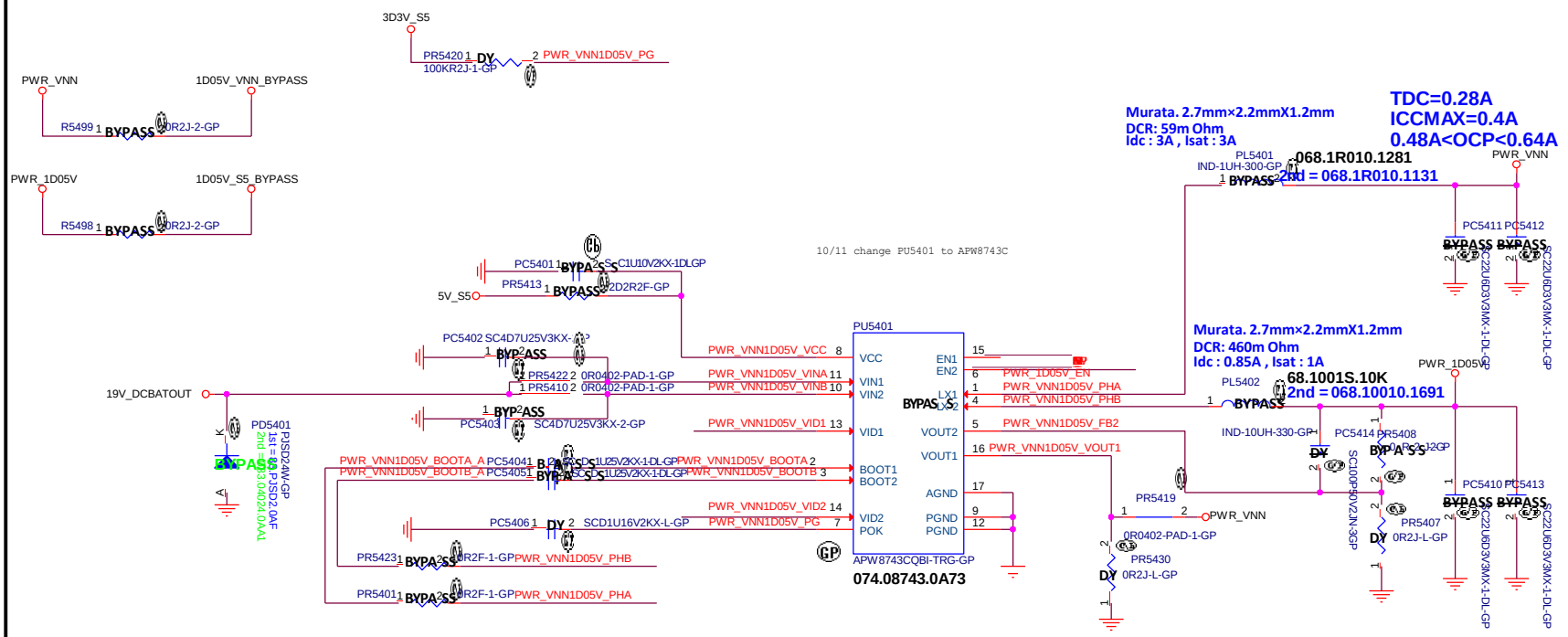
[40] PWR_1D05V_EN — PWR_1D05V_EN

PH on EE Side

1D05V_BYPASS_CTRL
[40] PWR_VNN1D05V_VID2 — PWR_VNN1D05V_VID2

PM_SLP_S3#
[40] PWR_VNN1D05V_VID1 — PWR_VNN1D05V_VID1

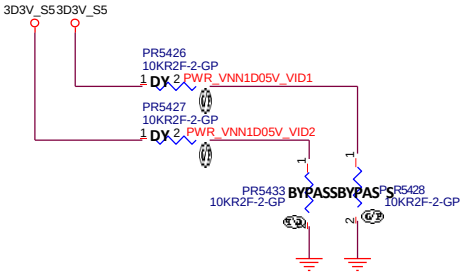
OFFPAGE-GAP



teknisi-indonesia.com

VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V



<Core Desiign>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER(APW8738A_VNN1D05)

Size: A3 | Document Number: HELLCAT_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 54 of 105

Main Func = LCD

INVERTER POWER

From CPU

[4] eDP_TX_CPU_N0
[4] eDP_TX_CPU_P0
[4] eDP_TX_CPU_N1
[4] eDP_TX_CPU_P1
[4] eDP_TX_CPU_N2
[4] eDP_TX_CPU_P2
[4] eDP_TX_CPU_N3
[4] eDP_TX_CPU_P3

[4] eDP_AUX_CPU_P
[4] eDP_AUX_CPU_N
[4] EDP_HPD
[4] eDP_VDD_EN
[4] L_BKLT_CTRL

From EC

[24] PANEL_BKEN
[17,40,81] SIO_SLP_S3#

20191023 Mao Lee (EVT1)
Follow Dell_CY20 change net name

FOR TESTING

[20] DBC_PANEL_EN
[24] LCD_VCC_TEST_EN
[24] LCD_TST
[24] CABLE2_OCP#
[24] PANEL_MONITOR
[66] 3D3V_LCDVDD_R
[20,70] SENSOR_I2C_SDA
[20,70] SENSOR_I2C_SCL
[20] GSEN_INT1_C

20191023 Mao Lee (EVT1)
Follow upsell change net name
add 0 ohm for debug

Touch Panel
Sensor
Camera
DMIC

Touch Panel
CCD& CAM
Sensor Board
Display
eDP

20200121 Mao Lee (DVT)
ADD R5571 R5573 R5574 R5575 R5576 R5577 R5578
For Colay 17"

LCD2 only for 17". Colay with LCD1

20200115 DVT1
For 17" Co-Layout

020.F0847.0040
2nd = 020.F1427.0040
3rd = 20.F2406.040

020.F1253.0050
2nd = 020.F0688.0050
3rd = 020.F0574.0050

Main Func = Touch panel

[20] I2C0_SDA_TS
[20] I2C0_SCL_TS
[20] TOUCH_PANEL_INTR#
[24] TOUCH_REPORT_SW
[20] TOUCH_PANEL_DET#
[3] TOUCH_PANEL_PD#

Hinge up cable protection

20191023(EVT1)
Follow Dell_CY20 change net name
20200420(DVT2)
Change C5542 to 0402 for layout limit

83.R2003.A8M
2ND = 083.52030.008F

074.02895.0A73

MIC POWER

CAMERA POWER

SENSOR POWER

TOUCH PANEL POWER

PANEL_PWRGD CIRCUIT

Brightness

EC (BIST MODE)

84.T3906.E11
2nd = 84.T3906.I11
3rd = 084.03906.0B11
4th = 084.03906.0C11

83.R2003.A8M
2ND = 083.52030.008F

84.T3904.H11
2nd = 84.03904.K11

Gen 10 LCD-BIST
Check if 3V and B+ is power on before doing panel self-test. It's using for judge MB or panel damaged.

Main Func = CAMERA

[16] CCD_USB20_N
[16] CCD_USB20_P
[27] DMIC_SCL_CODEC
[27] DMIC_SDA_CODEC
[19] DMIC_PCH_CLK_Q
[19] DMIC_PCH_DATA_Q

2020/02/29:swap EL5501

68.02002.061
2nd = 068.09002.2001

075.09904.0A7C

2020/02/29:swap RN5505

DY_DMICtoCODEC

<Core Design>

Wistron Corporation
23F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD&CAM&DMC&Touch
Size: Document Number: HELLCAT_TGL
Custom
Rev: A00
Date: Saturday, August 01, 2020
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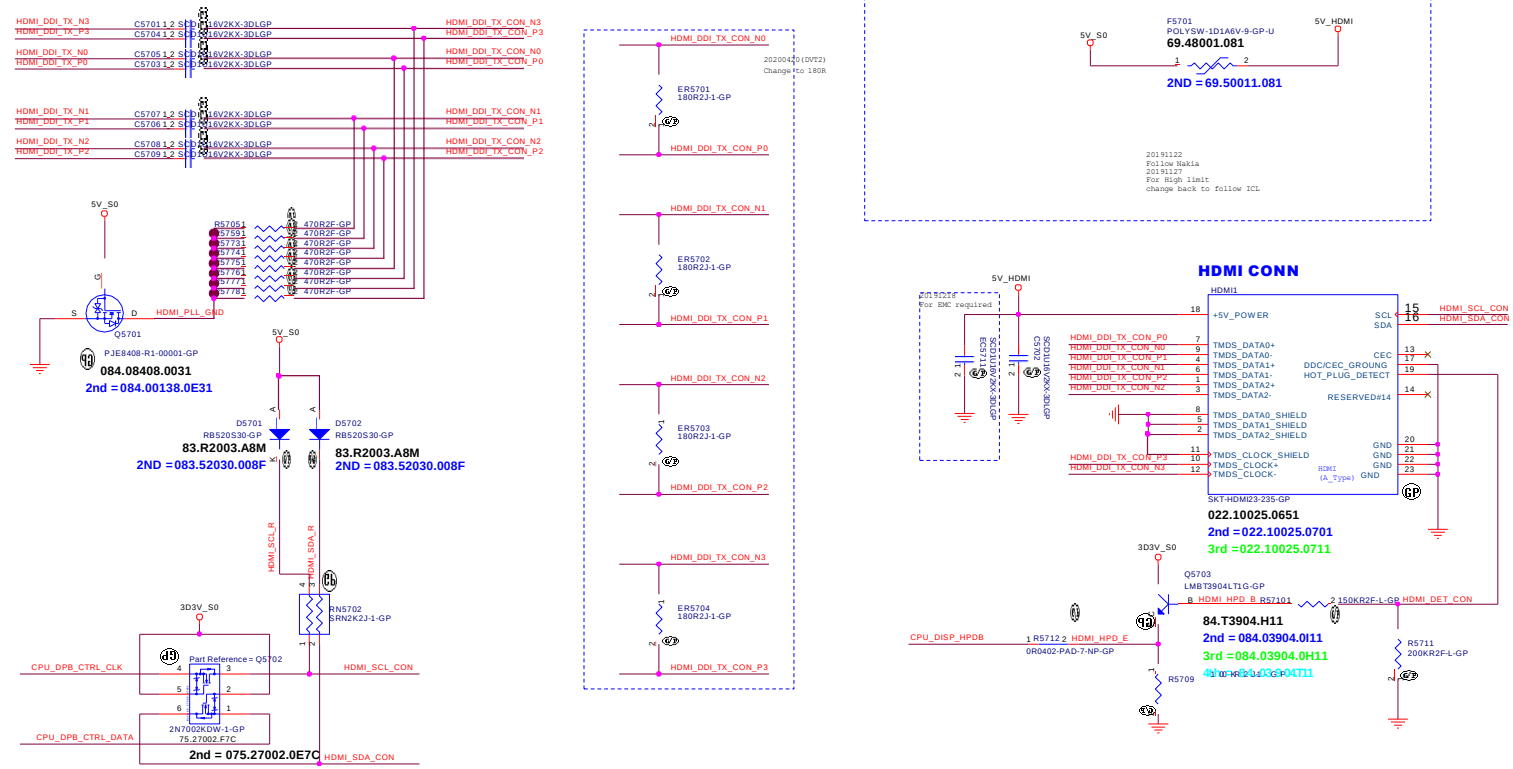
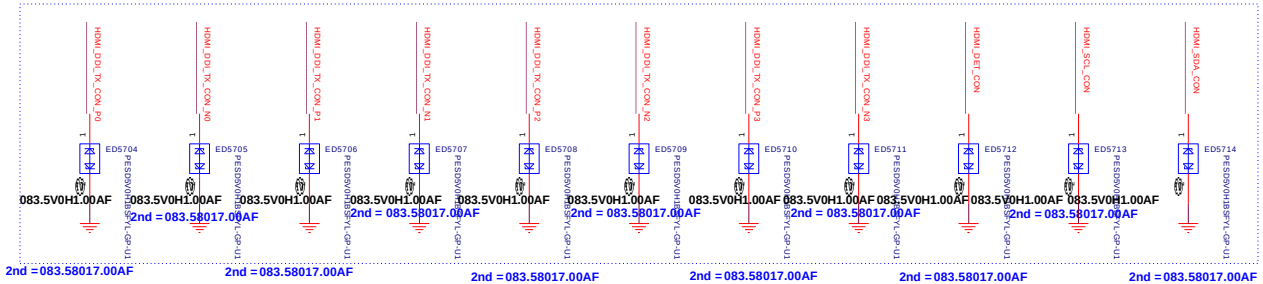
SSID = HDMI Level Shifter/Connector



EMI Request:



<Core Desiign>

Wistron Corporation
21F., 88, Sec.1, HsinTaiWu Rd., Hsichih,
TaipeiHsien 221, Taiwan, R.O.C.

Title: **HDMI**

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Main Func = WLAN

PCIE

[16] WLAN_PCIE_TX_N
[16] WLAN_PCIE_TX_P
[16] WLAN_PCIE_RX_N
[16] WLAN_PCIE_RX_P

PCIE_CLK

[18] WLAN_CLK_CPU_N
[18] WLAN_CLK_CPU_P
[18] CLK_PCIE_WLAN_REQ#

USB2.0

[16] BT_USB20_P
[16] BT_USB20_N

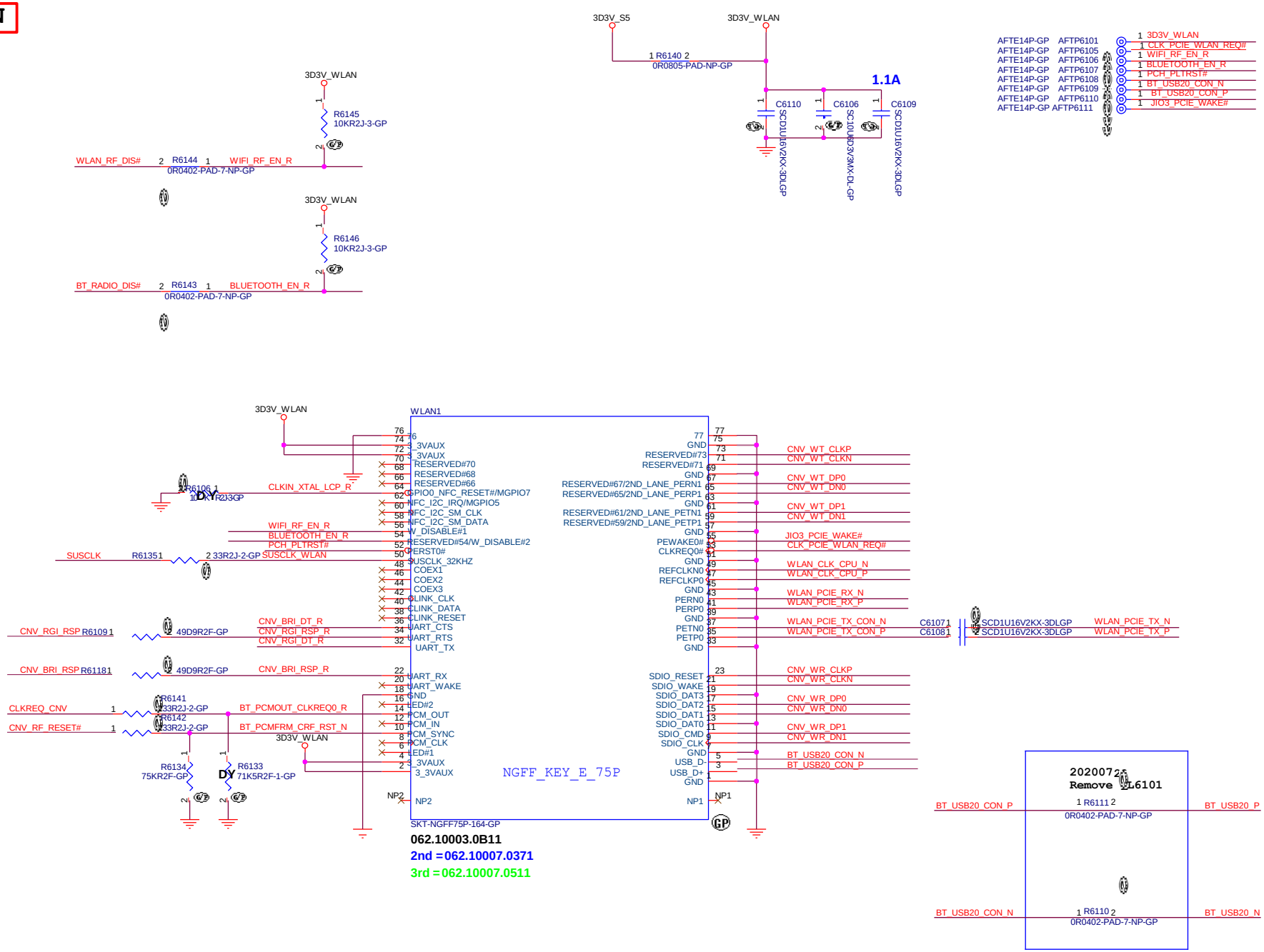
Single end

[19] BT_RADIO_DIS#
[16] WLAN_RF_DIS#
[17,63,66,71,76,91] PCH_PLTRST#
[18,24] SUSCLK

Debug

Power EN (Madesimo)

[21] CNV_BRI_DT_R
[21] CNV_RGI_DT_R
[21] CLKREQ_CNV
[21] CNV_RF_RESET#
[21] CNV_WT_DN0
[21] CNV_WT_DP0
[21] CNV_WT_DN1
[21] CNV_WT_DP1
[21] CNV_WT_CLKN
[21] CNV_WT_CLKP
[21] CNV_WR_DN0
[21] CNV_WR_DP0
[21] CNV_WR_DN1
[21] CNV_WR_DP1
[21] CNV_WR_CLKN
[21] CNV_WR_CLKP
[21] CNV_BRI_RSP
[21] CNV_RGI_RSP
[24] JIO3_PCIE_WAKE#



<Core Desiign>

Wistron Corporation
21F, 88, Sec.1, HsiinTaiiWu Rd., Hsiiichiih, Taiipeii-Hsiien221, Taiiiwan, R.O.C.

Title: NGFF WLAN CONN

Size: A3 | Document Number: HELLCAT_TGL | Rev: A00

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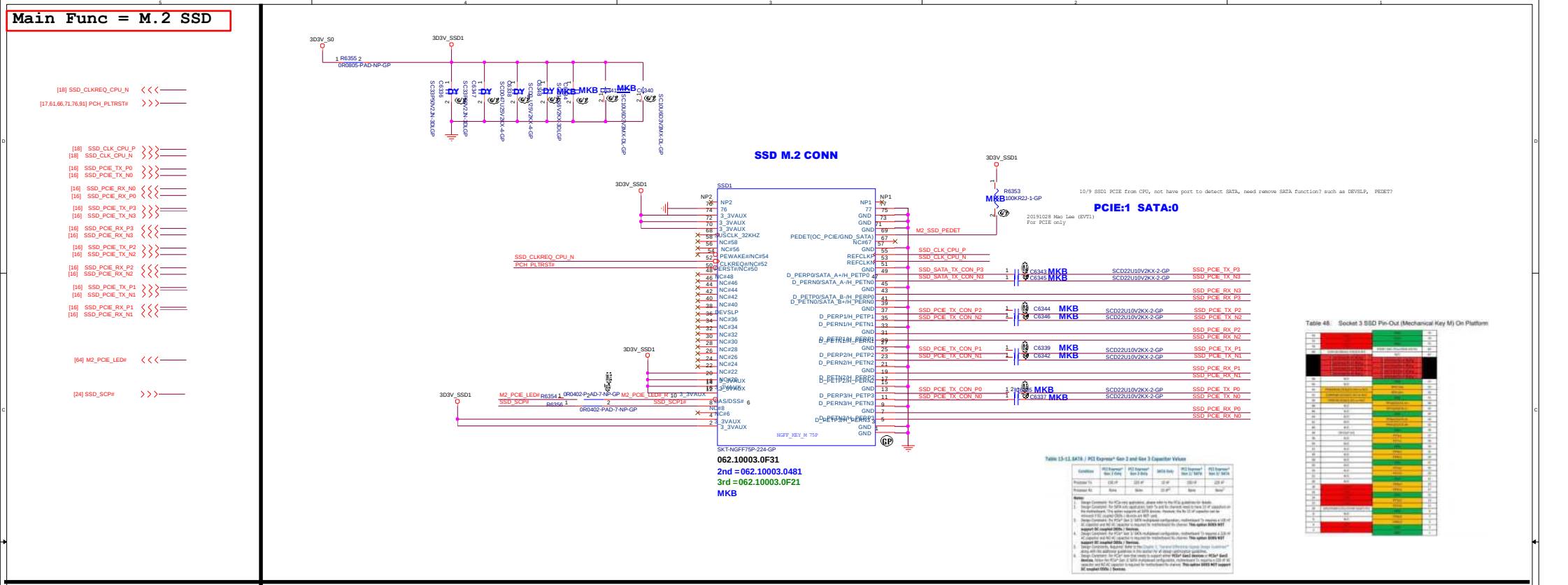
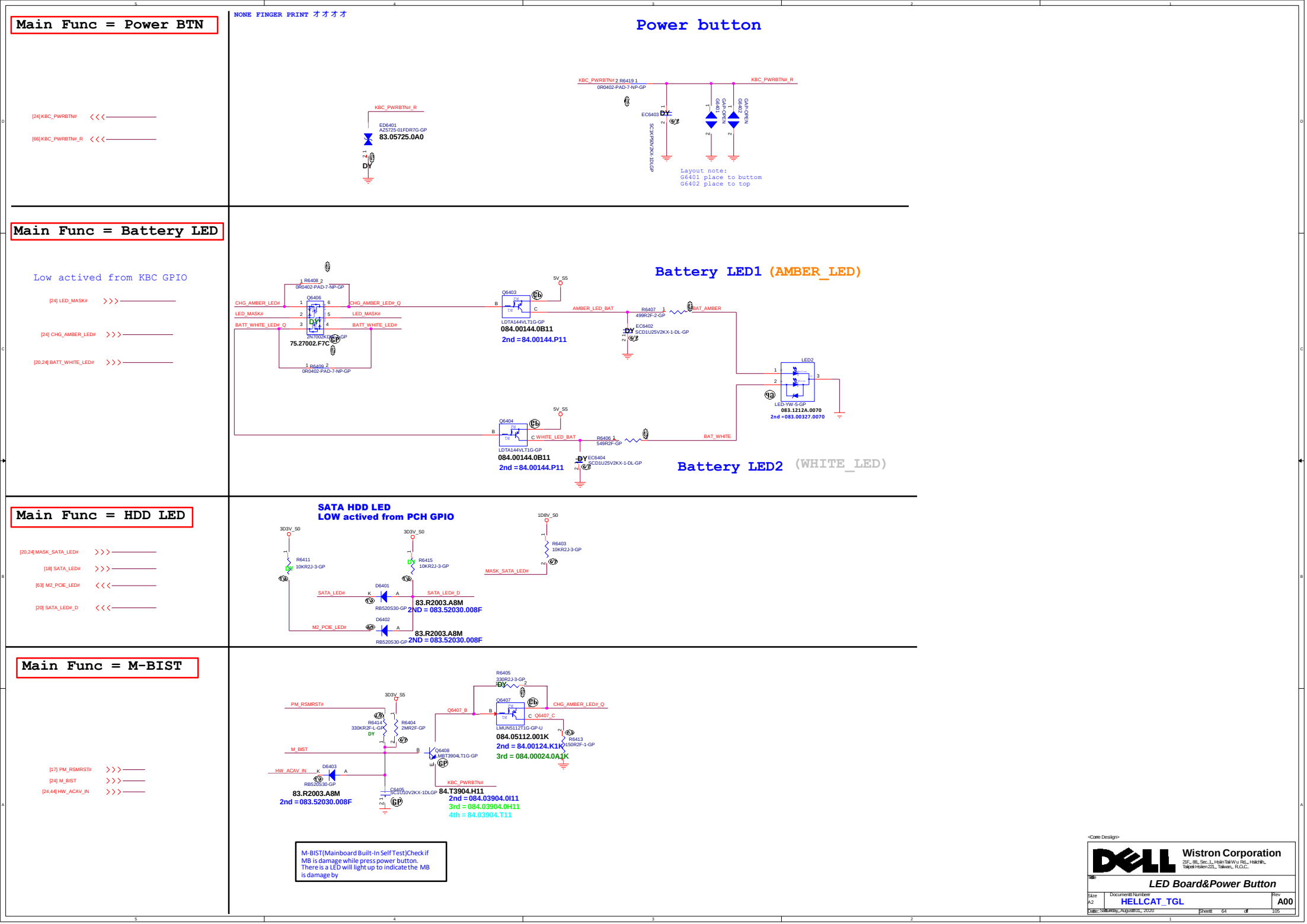
Main Func = M.2 SSD





Main Func = Power BTN
NONE FINGER PRINT オオオオ
Power button
[24] KBC_PWRBTN#
[66] KBC_PWRBTN#_R
KBC_PWRBTN#_R
ED6401
AZ5725-01FDR7G-GP
83.05725.0A0
KBC_PWRBTN# 2 R6419 1
0R0402-PAD-7-NP-GP
KBC_PWRBTN#_R
EC6403
SC1KP50V2KX-1DLGP
GAP-OPEN
G6401
G6402
Layout note:
G6401 place to buttom
G6402 place to top
Main Func = Battery LED
Low actived from KBC GPIO
[24] LED_MASK#
[24] CHG_AMBER_LED#
[20,24] BATT_WHITE_LED#
Battery LED1 (AMBER_LED)
R6408 2
0R0402-PAD-7-NP-GP
Q6406
CHG_AMBER_LED#
LED_MASK#
BATT_WHITE_LED#_Q
CHG_AMBER_LED#_Q
LED_MASK#
BATT_WHITE_LED#
2N7002KDW-GP
75.27002.F7C
R6409 2
0R0402-PAD-7-NP-GP
5V_S5
Q6403
LDTA144VLT1G-GP
084.00144.0B11
2nd = 84.00144.P11
AMBER_LED_BAT
R6407 1
499R2F-2-GP
BAT_AMBER
EC6402
SCD1U25V2KX-1-DL-GP
LED2
LED-YW-5-GP
083.1212A.0070
2nd = 083.00327.0070
5V_S5
Q6404
LDTA144VLT1G-GP
084.00144.0B11
2nd = 84.00144.P11
WHITE_LED_BAT
R6406 1
549R2F-GP
BAT_WHITE
EC6404
SCD1U25V2KX-1-DL-GP
Battery LED2 (WHITE_LED)
Main Func = HDD LED
[20,24] MASK_SATA_LED#
[18] SATA_LED#
[63] M2_PCIE_LED#
[20] SATA_LED#_D
SATA HDD LED
LOW actived from PCH GPIO
3D3V_S0
R6411
10KR2J-3-GP
3D3V_S0
R6415
10KR2J-3-GP
1D8V_S0
R6403
10KR2J-3-GP
MASK_SATA_LED#
D6401
SATA_LED#
SATA_LED#_D
RB520S30-GP
83.R2003.A8M
2ND = 083.52030.008F
D6402
M2_PCIE_LED#
RB520S30-GP
83.R2003.A8M
2ND = 083.52030.008F
Main Func = M-BIST
[17] PM_RSMRST#
[24] M_BIST
[24,44] HW_ACAV_IN
R6405
330R2J-3-GP
3D3V_S5
PM_RSMRST#
R6414
330KR2F-L-GP
R6404
2MR2F-GP
Q6407_B
Q6407
CHG_AMBER_LED#_Q
Q6407_C
LMUN5112T1G-GP-U
084.05112.001K
2nd = 84.00124.K1K
3rd = 084.00024.0A1K
R6413
150R2F-1-GP
M_BIST
Q6408
MBT3904LT1G-GP
HW_ACAV_IN
D6403
RB520S30-GP
83.R2003.A8M
2nd = 083.52030.008F
C6405
SC1U10V2KX-1DLGP
KBC_PWRBTN#
84.T3904.H11
2nd = 084.03904.0I11
3rd = 084.03904.0H11
4th = 84.03904.T11
M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by
<Come Design>
Wistron Corporation
21F., 88., Sec. 1., Hsin Tai Wu Rd., Hsichih., Taipei Hsien 221., Taiwan., R.O.C.
Title
LED Board&Power Button
Size
A2
Document Number
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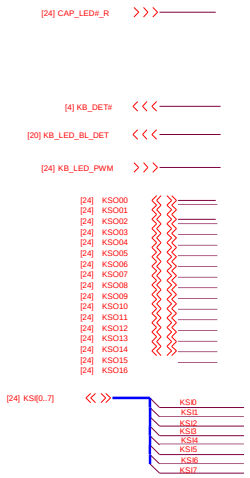
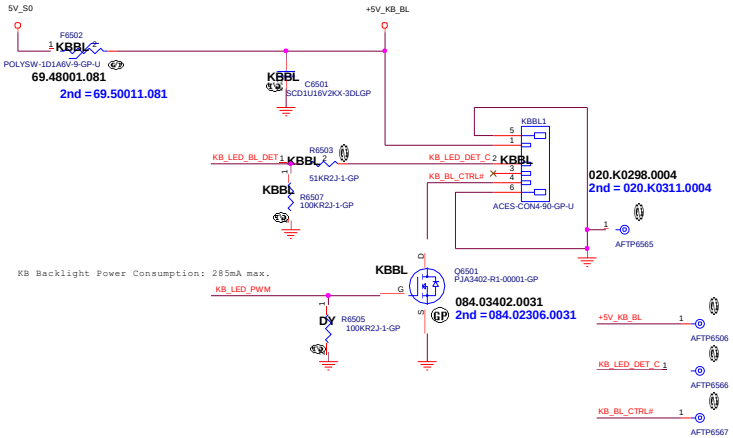
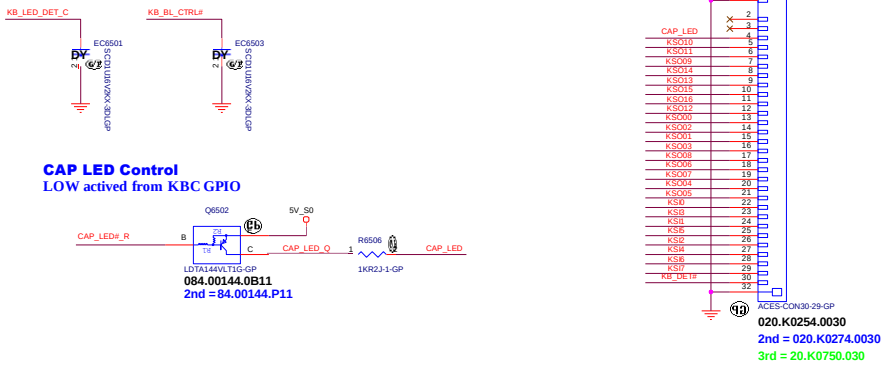
Main Func = KB



Keyboard Backlight (Reserved)



Internal Keyboard Connector

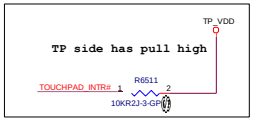


CAP LED Control

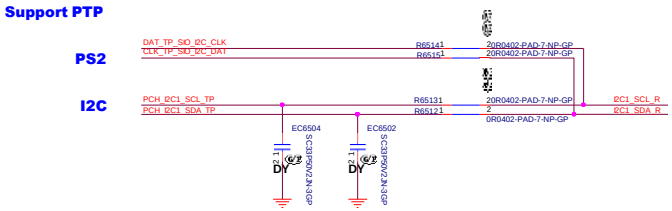
LOW actived from KBC GPIO

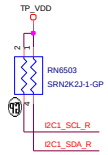
Main Func = TPAD

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

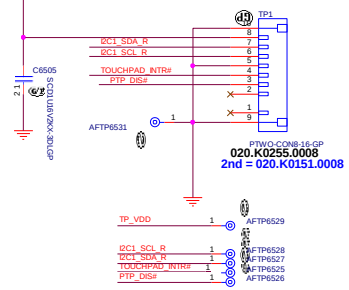


Support PTP





Precision Touch Pad Connector



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

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Title: Key Board&Touch Pad

Size: A2 | Document Number: HELLCAT_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 65 of 105

Main Func = IO Connector

AUDIO

[27,29] AUD_RING
[27,29] AUD_SLEEVE
[29] AUD_HP1_JACK_L1
[29] AUD_HP1_JACK_R1
[27] AUD_SENSE

CRD

[16] CARD1_USB20_N
[16] CARD1_USB20_P
[18] HDST_SO_WP#

USB3.0

PORT1

[16] USB2_USB30_RX_N
[16] USB2_USB30_RX_P
[16] USB2_USB30_TX_N
[16] USB2_USB30_TX_P
[16] USB2_USB20_N
[16] USB2_USB20_P

USB CONTROL

[4] USB_OC1#
[24,35] USB_PWR_EN#

LAN

[16] LAN_PCIE_RX_N
[16] LAN_PCIE_RX_P
[16] LAN_PCIE_TX_N
[16] LAN_PCIE_TX_P
[18] LAN_CLK_CPU_N
[18] LAN_CLK_CPU_P
[18] CLK_PCIE_LAN_REQ#
[26] PM_LAN_ENABLE
[24] PCIE_LAN_WAKE#

FP

[16] FP1_USB20_N
[16] FP1_USB20_P
[24] FPR_SCAN#
[64] KBC_PWRBTN#_R
[17,51] SIO_SLP_S4#

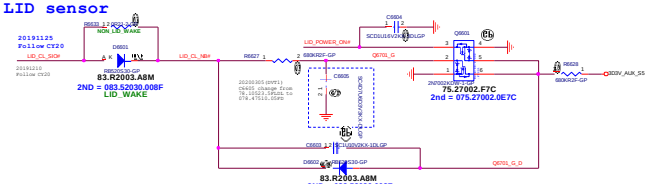
[20,24] LID_CL_SIO#
[24] LID_POWER_ON#
[20,24] LID_CL_SIO_TAB#
[17,61,63,71,76,91] PCH_PLTRST#
[20,69] PCH_I2C1_SCL_TP
[20,69] PCH_I2C1_SDA_TP
[44] PWR_CHG_VBATIN
[55] 3D3V_LCDVDD_R

USB2.0 Power

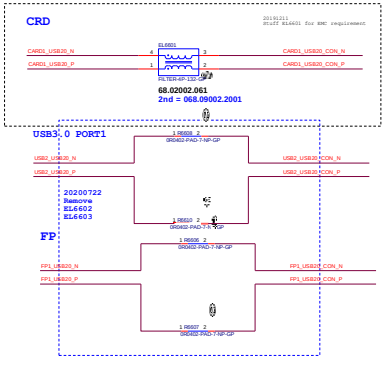
Pin define by follow layout routing

074.00524.0C9F
2nd = 074.03553.007G
3rd = 074.09742.009F

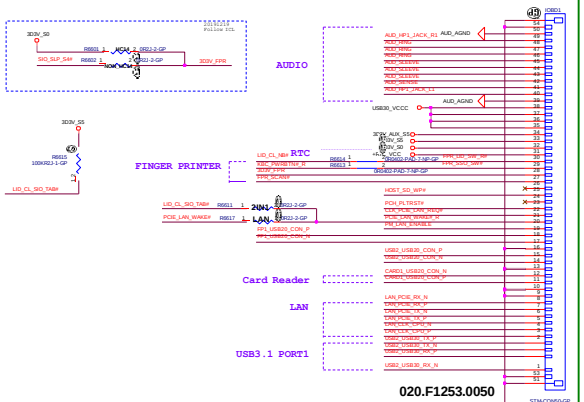
LID sensor



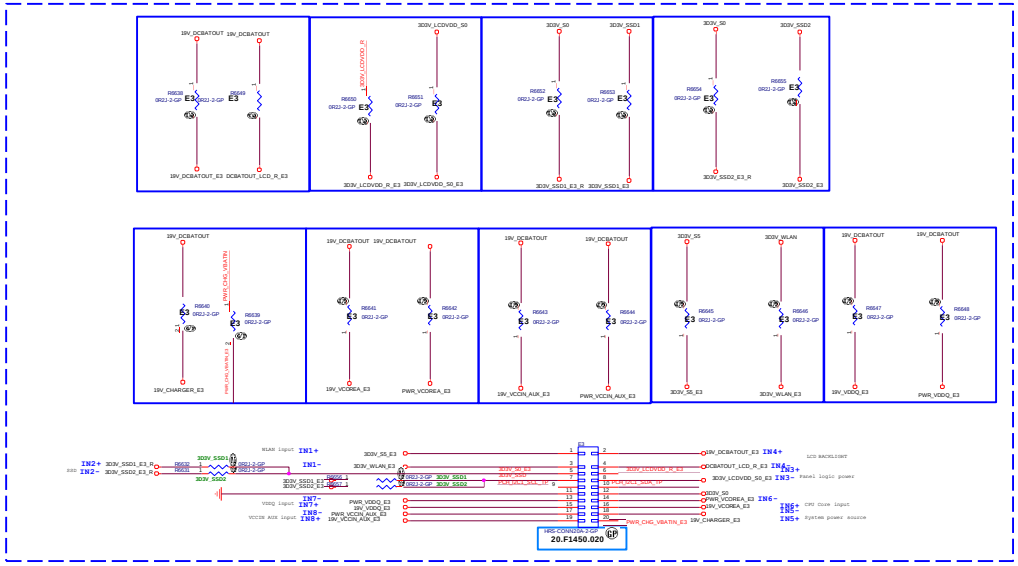
CRD



I/O Board Connector



020.F1253.0050
2nd = 020.F0688.0050
3rd = 020.F0574.0050



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IO Board Connector

Size	Document Number	Rev
A1	HELLCAT_TGL	A00

Date: Monday, August 31, 2020 Sheet 2 of

Main Func = Debug

ESPI

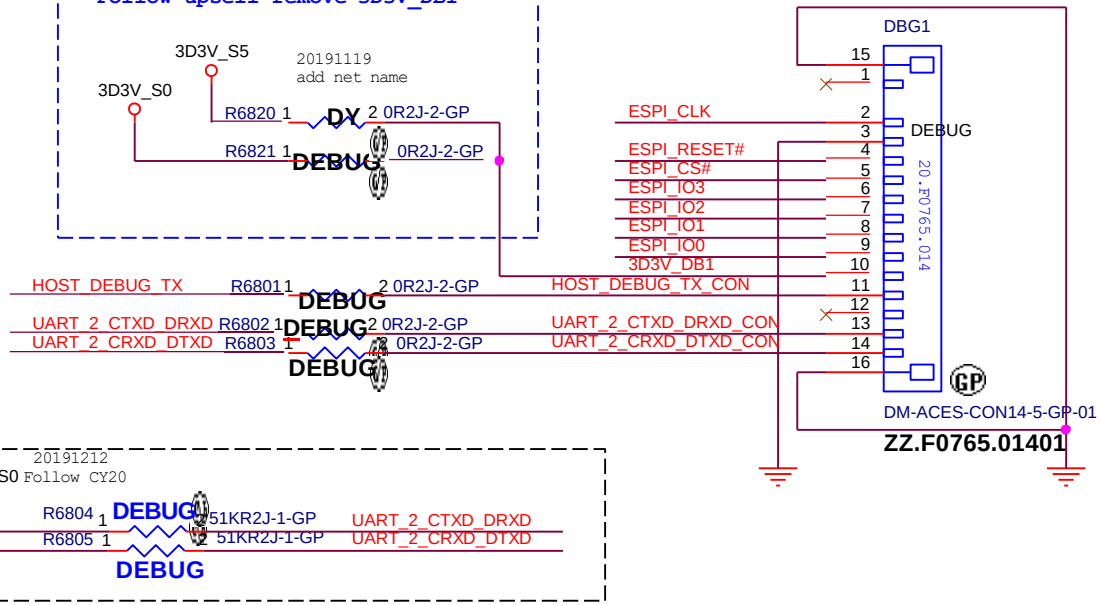
[18,24] ESPI_CLK
[18,24] ESPI_RESET#
[18,24] ESPI_CS#

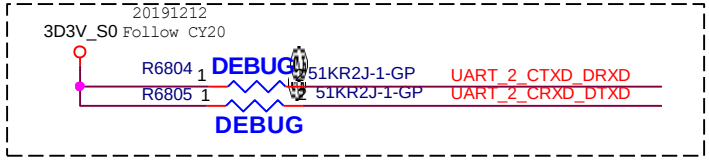
[18,24] ESPI_IO0
[18,24] ESPI_IO1
[18,24] ESPI_IO2
[18,24] ESPI_IO3

UART

[24] HOST_DEBUG_TX
[20] UART_2_CTXD_DRXD
[20] UART_2_CRXD_DTXD

ESPI Debug Connector





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Title: *Dubug connector*		
Size: A4	Document Number: *HELLCAT_TGL*	Rev: *A00*
Date: Saturday, August 01, 2020	Sheet 68 of 105	

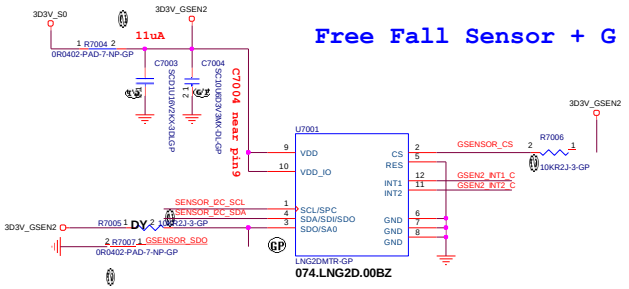
SSID = User.interface

Mantis Accelerometer for adaptive thermal and HDD protection

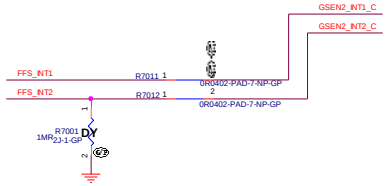
The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

[20] GSEN2_INT1_C
[20,55] SENSOR_I2C_SCL
[20,55] SENSOR_I2C_SDA
[20] FFS_INT1
[19] FFS_INT2

Free Fall Sensor + G Sensor



HellCat using 8 Bits:074.LNG2D.00BZ
Mocking Bird using 12 Bits
:074.LIS2D.M002



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

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Title: Free Fall Sensor

Size	Document Number	Rev
A2	HELLCAT_TGL	A00

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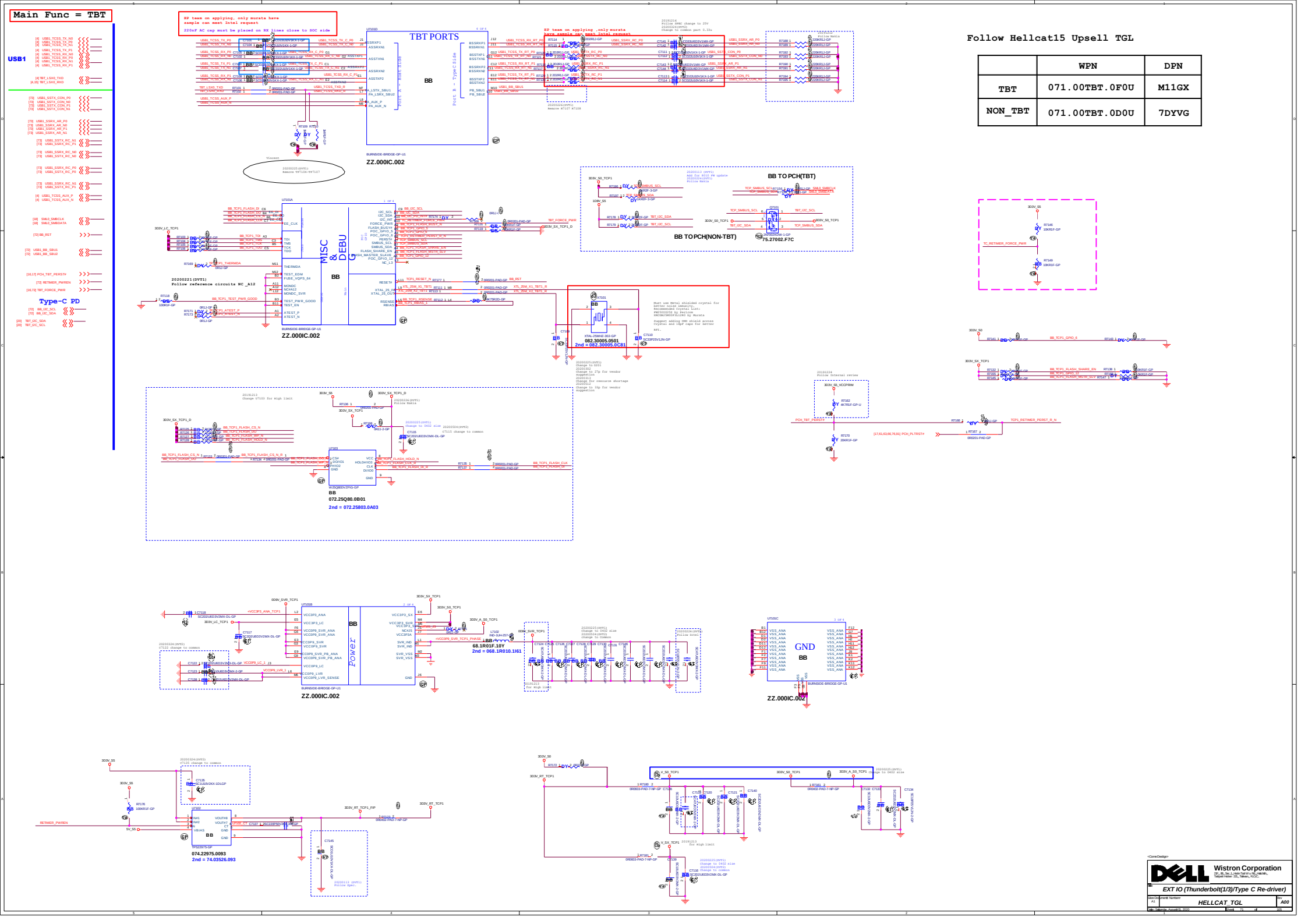

Follow Hellcat15 Upsell TGL

	WPN	DPN
TBT	071.00TBT.0F0U	M11GX
NON_TBT	071.00TBT.0D0U	7DYVG

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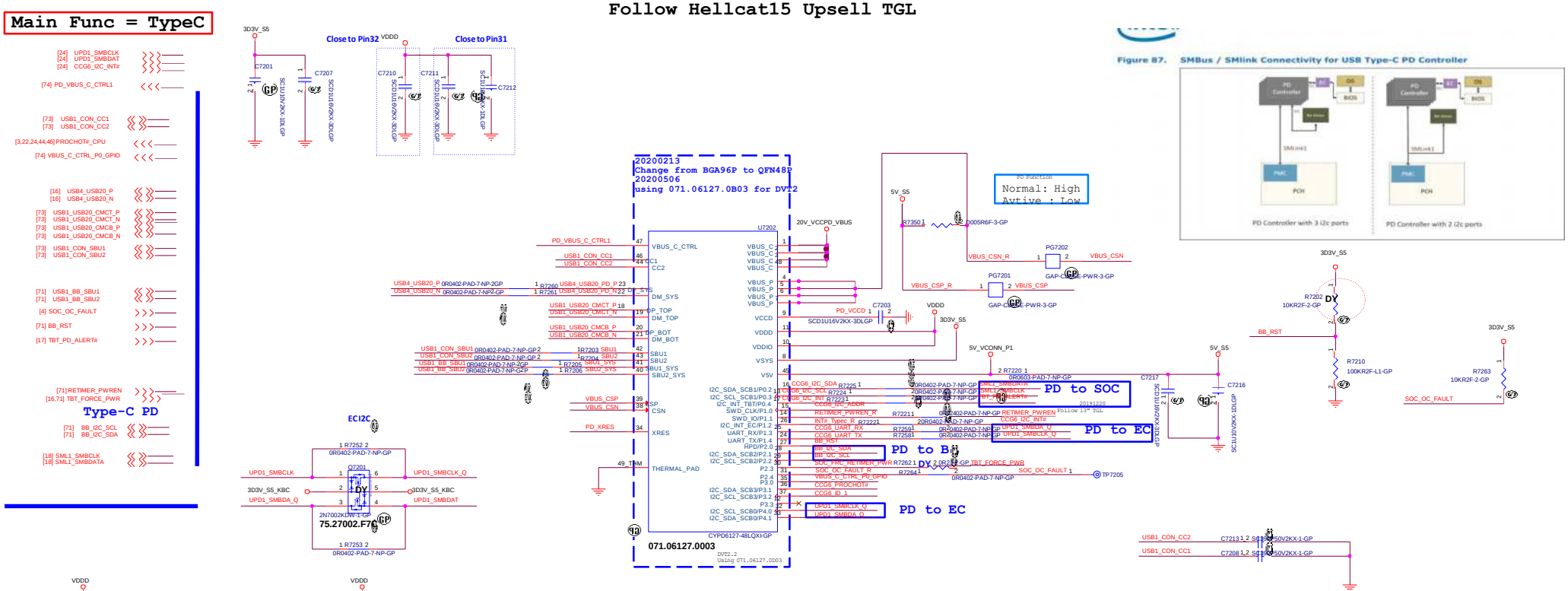
EXT IO (Thunderbolt(1/3)/Type C Re-driver)

HELLCAT_TGL

A00

Follow Hellcat15 Upsell TGL



Dell TGL Platform MOD_ID Options			
MUX	MOD_ID1	MOD_ID2	Description
BB8040R	L0	N/A	TBT Configuration w/BB Retimer
BB8010R	L2	N/A	non-TBT Configuration w/BB Retimer
TUSB546/1046	L6	L0	TUSB546 Equalizer config #1
TUSB546/1046	L6	L1 - L3	Reserved for TUSB546 Equalizer config #2,3,4 reserved

	CCG6_ID	R7216	R7218	計算值	理論值
0/8	L0	DY	64.10035.6DL (100K)	0	0
1/8	L1	064.71535.06D1 (715K)	64.10035.6DL (100K)	0.123	0.125
2/8	L2	64.30035.6DL (300K)	64.10035.6DL (100K)	0.25	0.25
3/8	L3	64.20035.6DL (200K)	64.12035.6DL (120K)	0.375	0.375
4/8	L4	64.10035.6DL (100K)	64.10035.6DL (100K)	0.5	0.5
5/8	L5	64.10035.6DL (100K)	64.20035.6DL (200K)	0.625	0.625
6/8	L6	64.22035.6DL (220K)	64.59035.6DL (590K)	0.728	0.75
7/8	L7	64.10035.6DL (100K)	064.71535.06D1 (715K)	0.877	0.875

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EXT IO (Thunderbolt(2/3)/Type C CC Logic)

HELLCAT_TGL

A00

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Main Func = TypeC

USB1

[71] USB1_SSTX_CON_P0
[71] USB1_SSTX_CON_N0
[71] USB1_SSTX_CON_P1
[71] USB1_SSTX_CON_N1

[71] USB1_SSRX_AR_P0
[71] USB1_SSRX_AR_N0
[71] USB1_SSRX_AR_P1
[71] USB1_SSRX_AR_N1

[72] USB1_USB20_CMCT_P
[72] USB1_USB20_CMCT_N
[72] USB1_USB20_CMCB_P
[72] USB1_USB20_CMCB_N

[72] USB1_CON_CC1
[72] USB1_CON_CC2

[72] USB1_CON_SBU1
[72] USB1_CON_SBU2

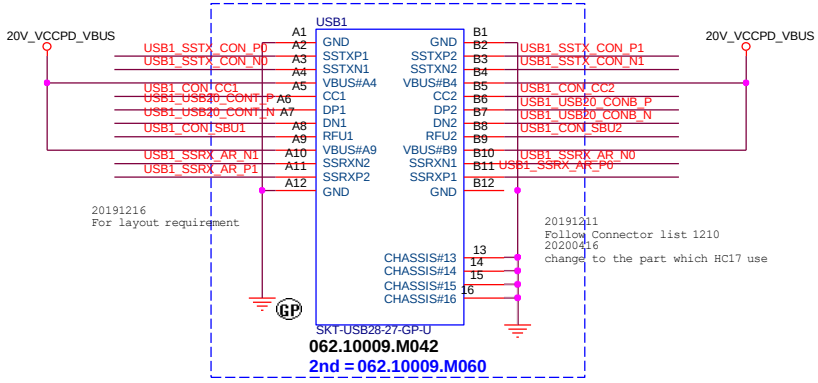
[71] USB1_SSTX_RC_N1
[71] USB1_SSRX_RC_P1

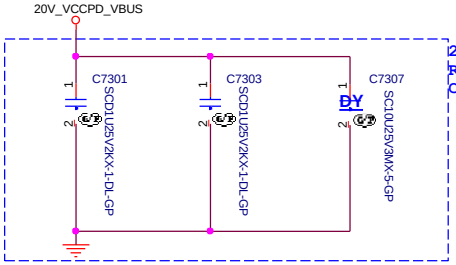
[71] USB1_SSRX_RC_N0
[71] USB1_SSTX_RC_N0

[71] USB1_SSRX_RC_P0
[71] USB1_SSTX_RC_P0

[71] USB1_SSRX_RC_N1
[71] USB1_SSTX_RC_P1

Follow Hellcat15 Upsell TGL

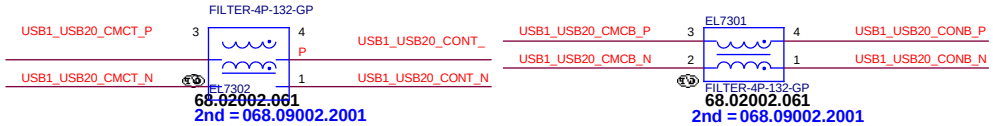




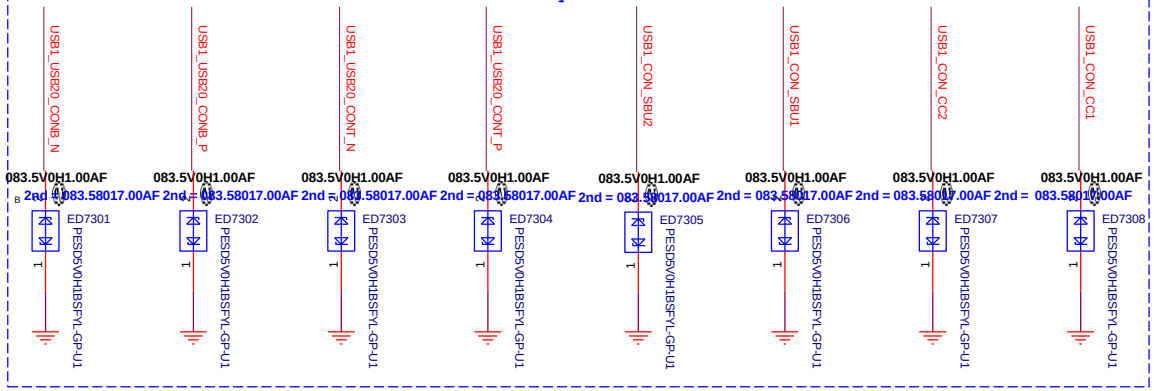
20200504
Remove C7302 C7304
Change C7301 C7302 to 0402 size

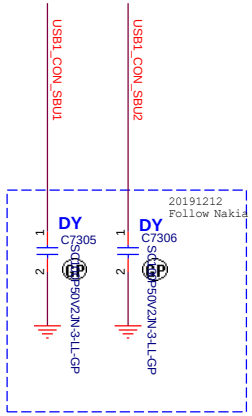
2020/02/29:swap EL7302/EL7301

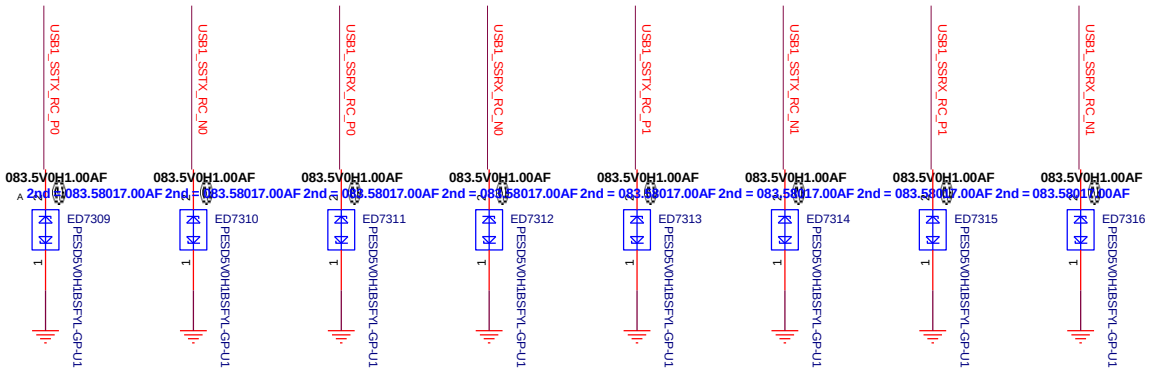
20200722
Remove R7301
R7302 R7303 R7304



20200213
Follow EMC requestment







<Core Desiign>

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Title: EXT IO (Thunderbolt(3/3)/Type C Conn)

Size	Document Number	Rev
A3	HELLCAT_TGL	A00

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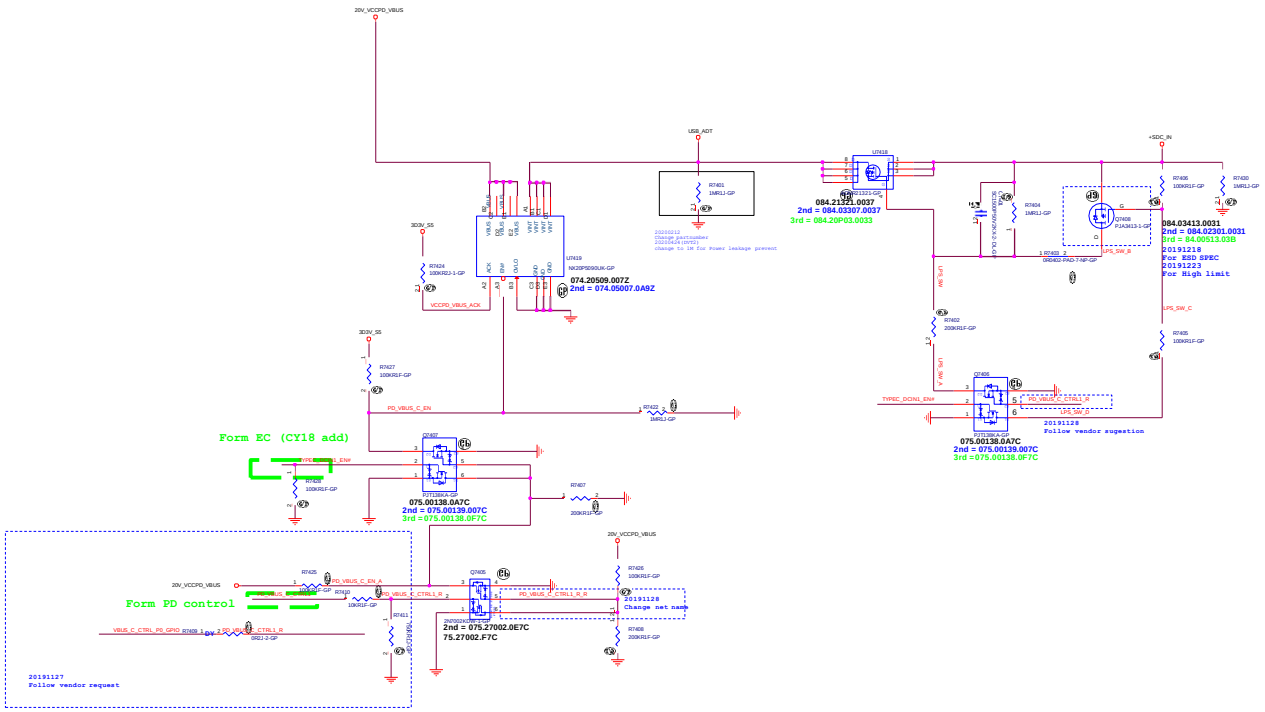
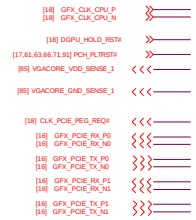
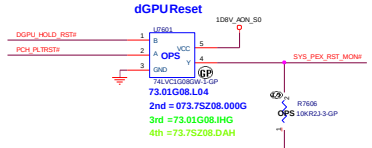
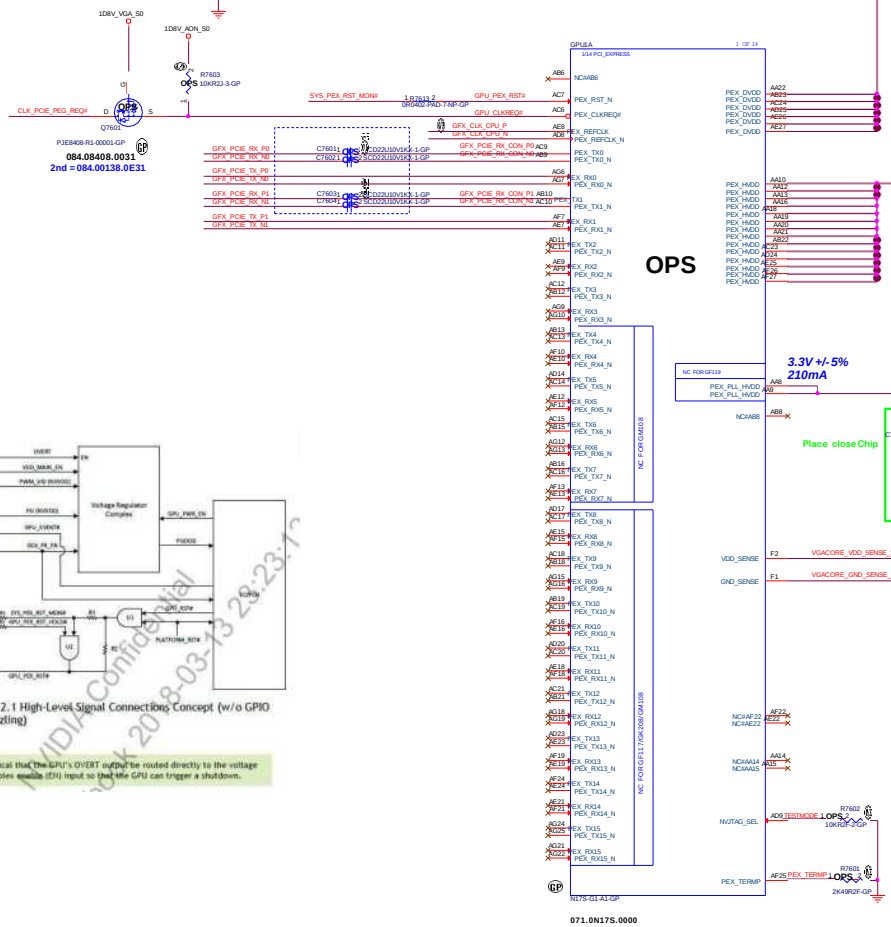
[73] PD_VBUS_C_CTRL1
[24] TYPEC_DCIN1_ENF
[44] VCCPD_VBUS_ACK
[72] VBUS_C_CTRL_PD_GPIO



Main Func = dGPU







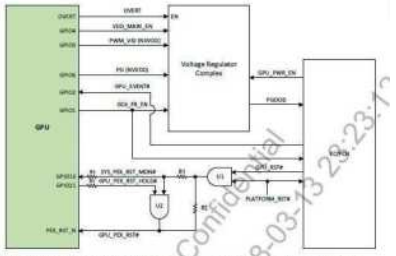


Figure 11. GC6 2.1 High-Level Signal Connections Concept (w/o GPIO Swizzling)

Note: It is critical that the GPU's OVERT output be routed directly to the voltage regulator complex enable (EN) input so that the GPU can trigger a shutdown.

POWER IC

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
PEX_PLL_HVDD Supply Rail					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU

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Friday, 2018-03-13 23:23:12

Kaori Confidential
Friday, September 07, 2018

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Title: GPU(1/5)PEG

Size: Document Number: HELLCAT_TGL Rev: A00

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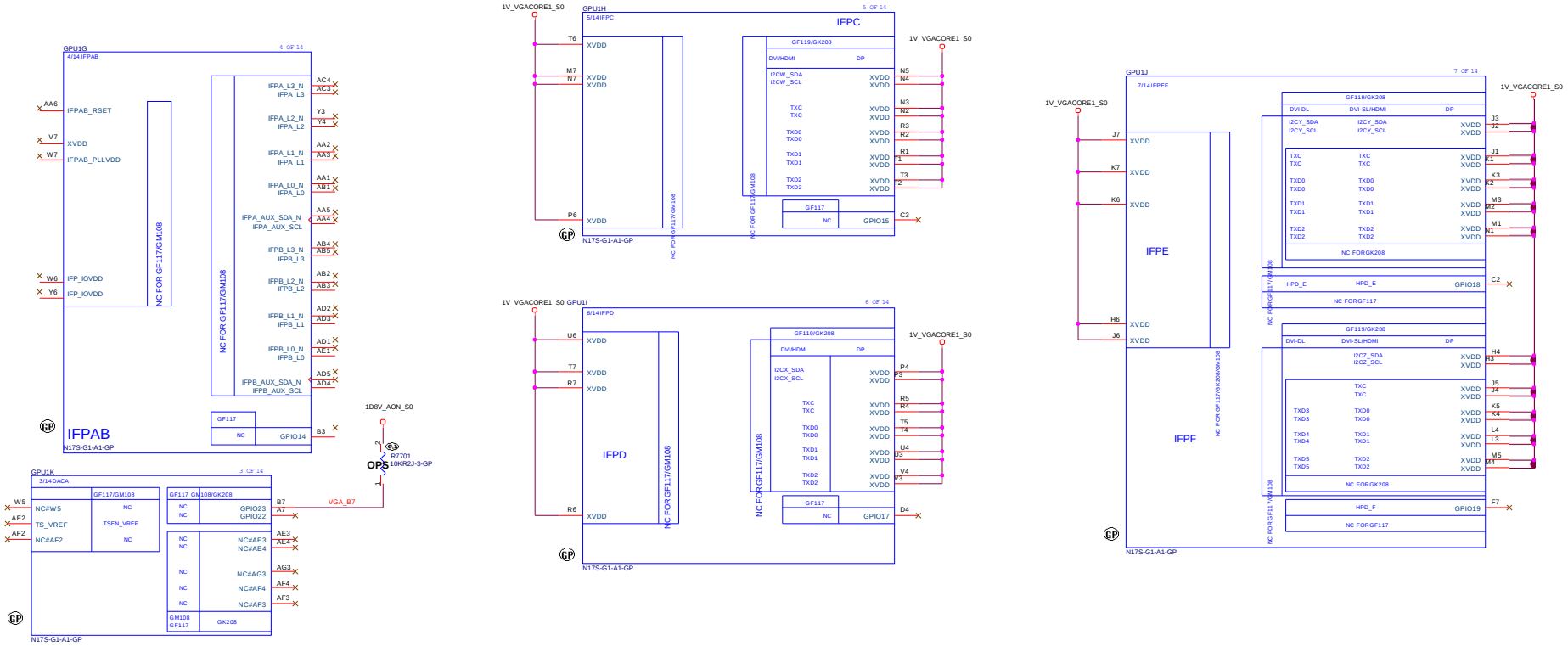
Main Func = dGPU



<Core Desiign>

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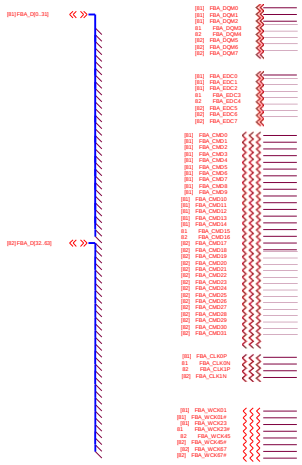
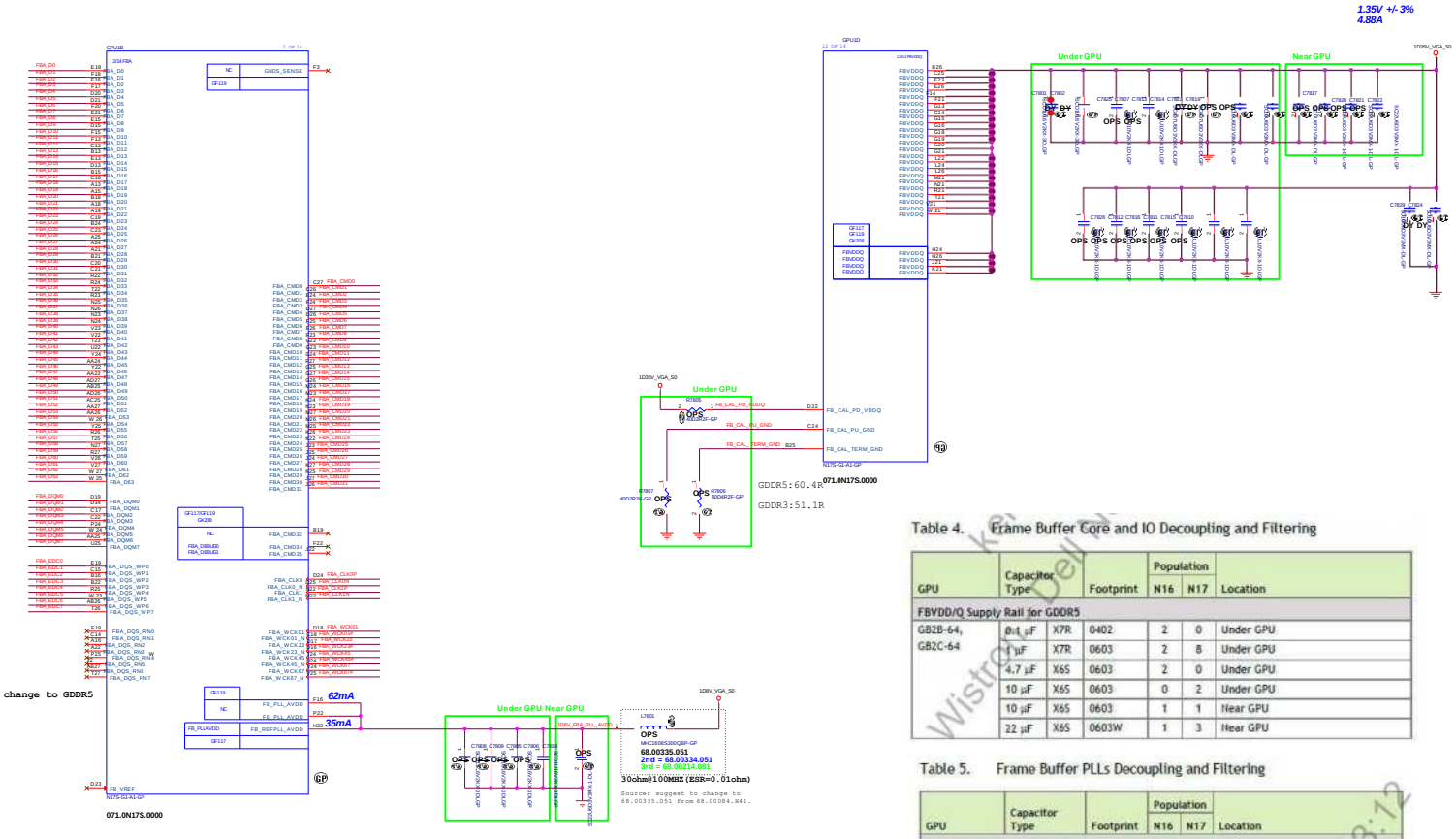
Title: ***GPU(2/5)DIGITALOUT***

Size	Document Number	Rev
A2	HELLCAT_TGL	A00

Date: Saturday, August 01, 2020 Sheet 77 of 105

Main Func = dGPU





Note:
Reference NV-DDR5 CRB and DOH70 by GDDR5

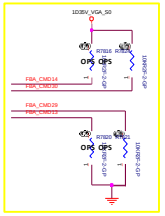


Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

<Core Design>

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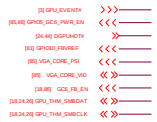
22F, 88,Sec.1,Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan., R.O.C.

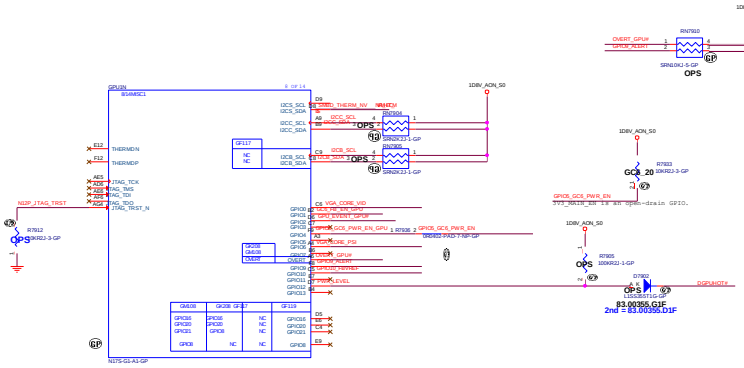
Title: GPU(3/5)VRAMI/F

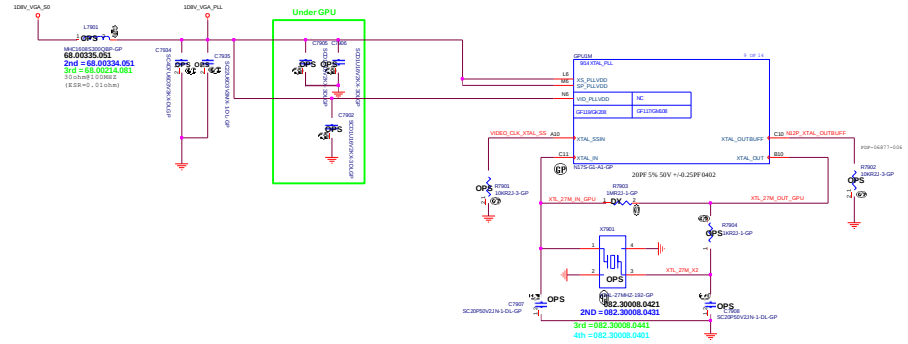
Size: Document Number: HELLCAT_TGL Rev: A00

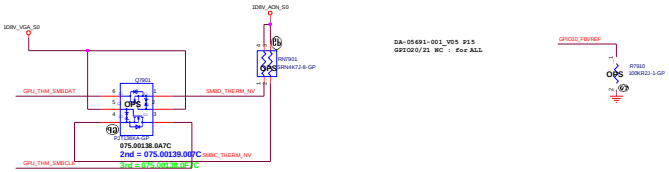
Date: Saturday, August 13, 2011 Sheet 78 of 105

Main Func = dGPU









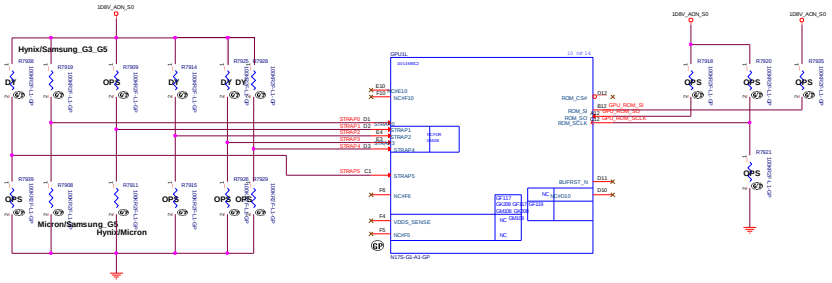


Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_DO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
1	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Table 6. N17S-G0/G2/G3/G4 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x7	8 Gbps	N/A	Full	Production ready
			Hynix	H9GQ2H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FC-HC25	C-die	0x3	8 Gbps	N/A	Full	Post-production ready

Notes:
1. For N17S-G0/G2/G3/G4, the maximum allowable memory case temperature is 85 °C.
2. N17S-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations in Table 5 for N17S-G1.

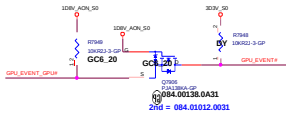
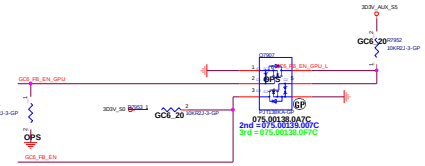


Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)



Neil for NVIDIA Corp. 2016-08-09
Neil for NVIDIA Corp. 2016-01-08
Chang Wei Chen

Core Design
Wistron Corporation
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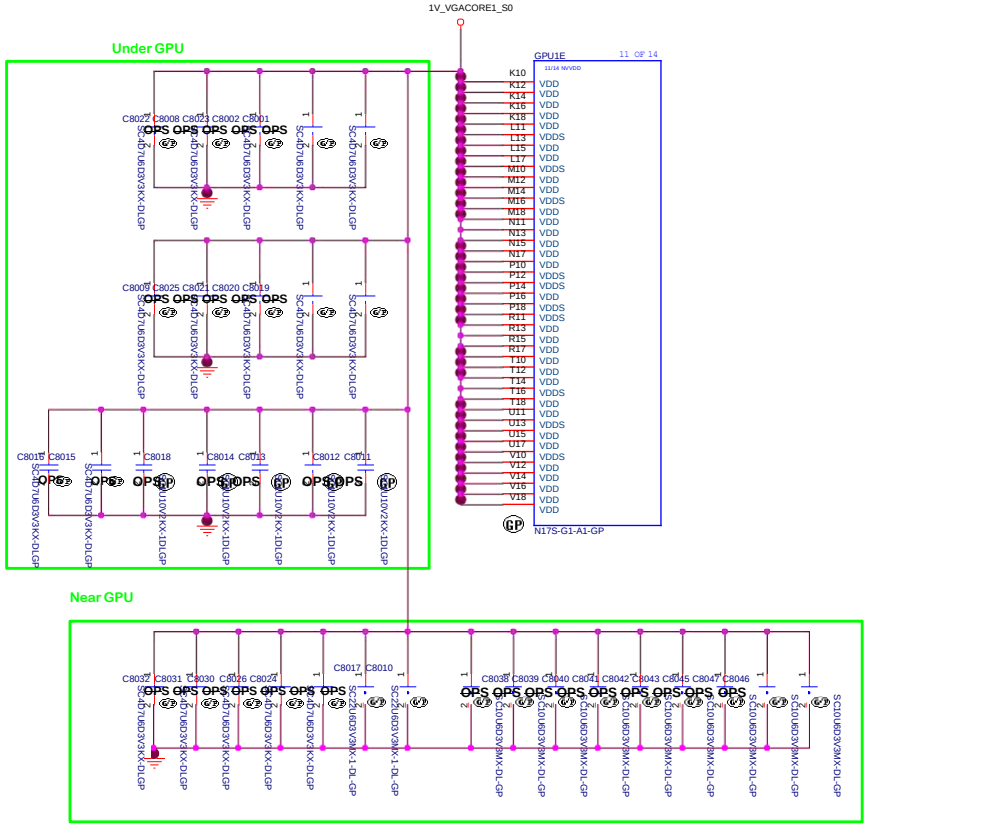
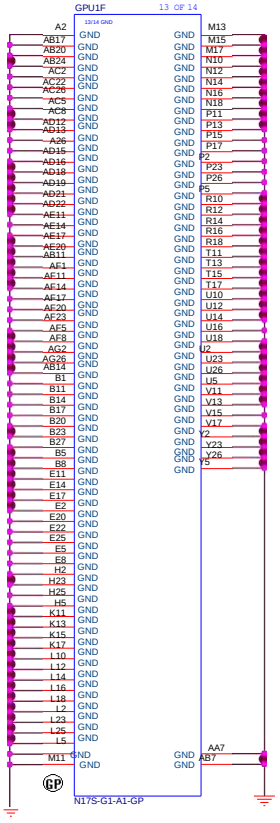
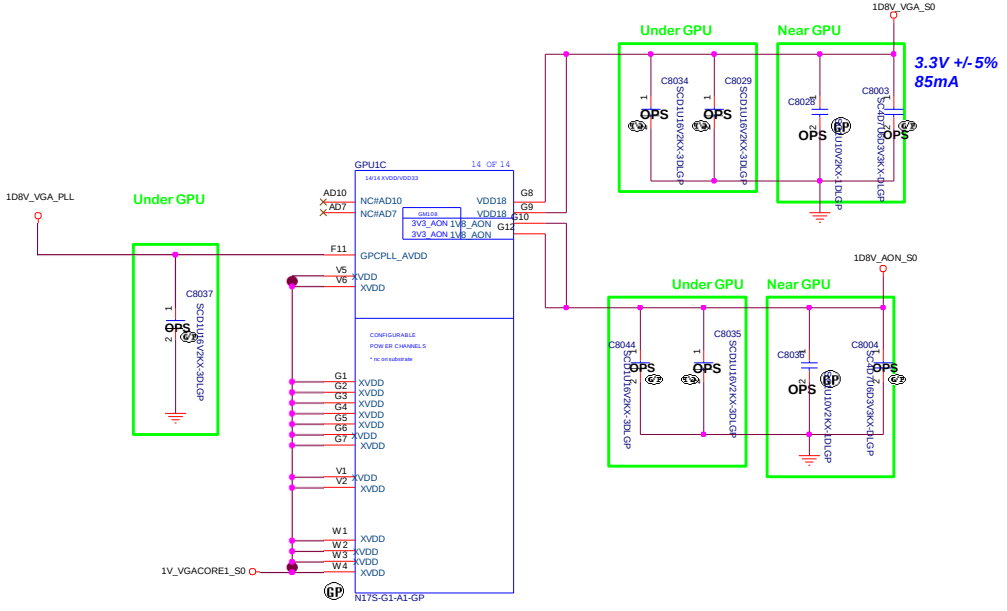
Title: GPU(4/5)GPIO/STRAP
Size: Document Number: HELLCAT_TGL
Rev: A00
Date: Wednesday, August 16, 2017
Sheet 78 of 102

Main Func = dGPU







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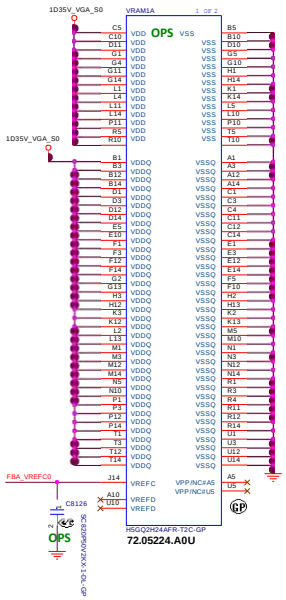
Title: GPU(5/5)PWR/GND

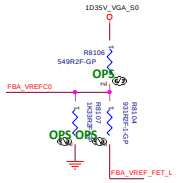
Size	Document Number	Rev
Custom	HELLCAT_TGL	A00

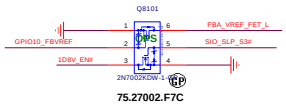
Date: Saturday, August 01, 2020 Sheet 80 of 105

SSID = VRAM



Frame Buffer Patition A-Lower Half

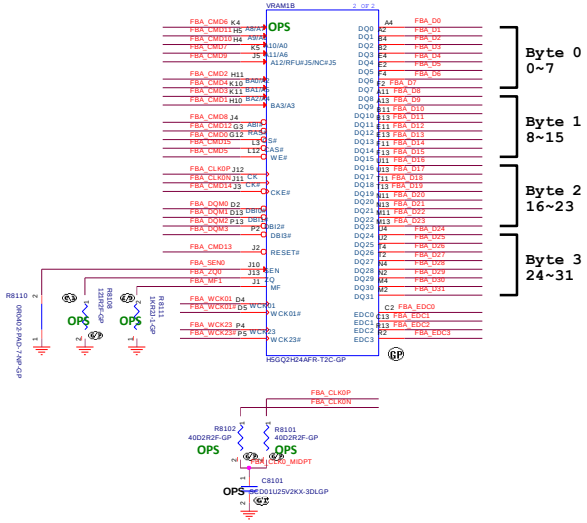


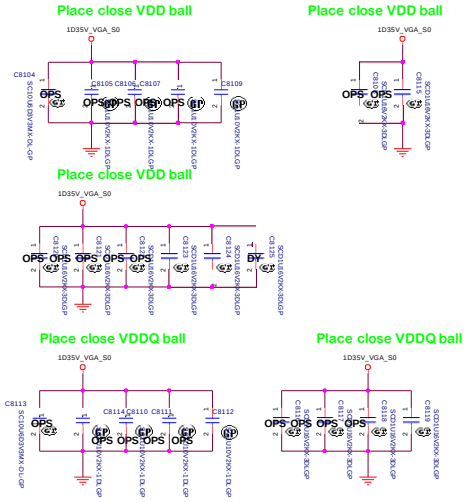


FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

Normal(MF=0)





<Core Design>

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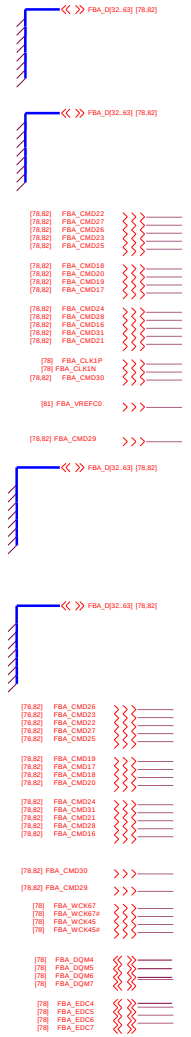
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM1,2 (1/4)**

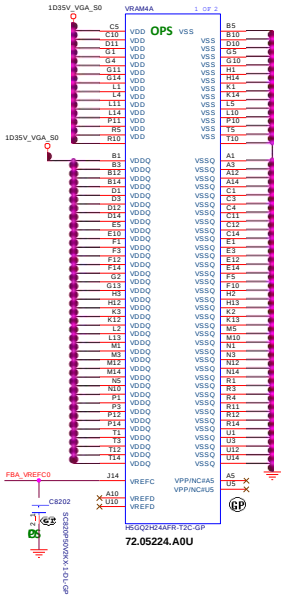
Size: Document Number: Custom — **HELLCAT_TGL** — Rev: **A00**

Date: Saturday, August 01, 2020 — Sheet 81 of 105

SSID = VRAM

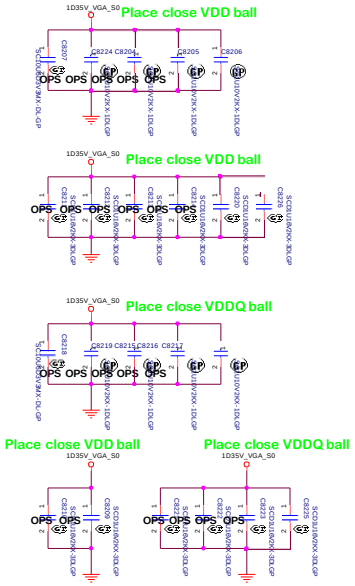


Frame Buffer Patition A-Upper Half

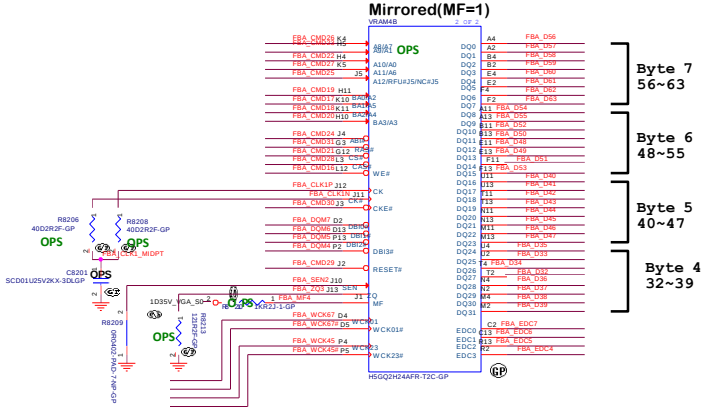


FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



Mirrored(MF=1)



<Core Design>

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Title: GPU-VRAM3.4 (2/4)

Size: Document Number: Custom — HELLCAT_TGL — Rev: A00

Date: Saturday, August 01, 2020 — Sheet 82 of 105

RT8816B For NVVDDS

VGA : N17S-G3/G5
EDP-Peak : 69.9A

OFFPAGE-Signal

PH on EE side

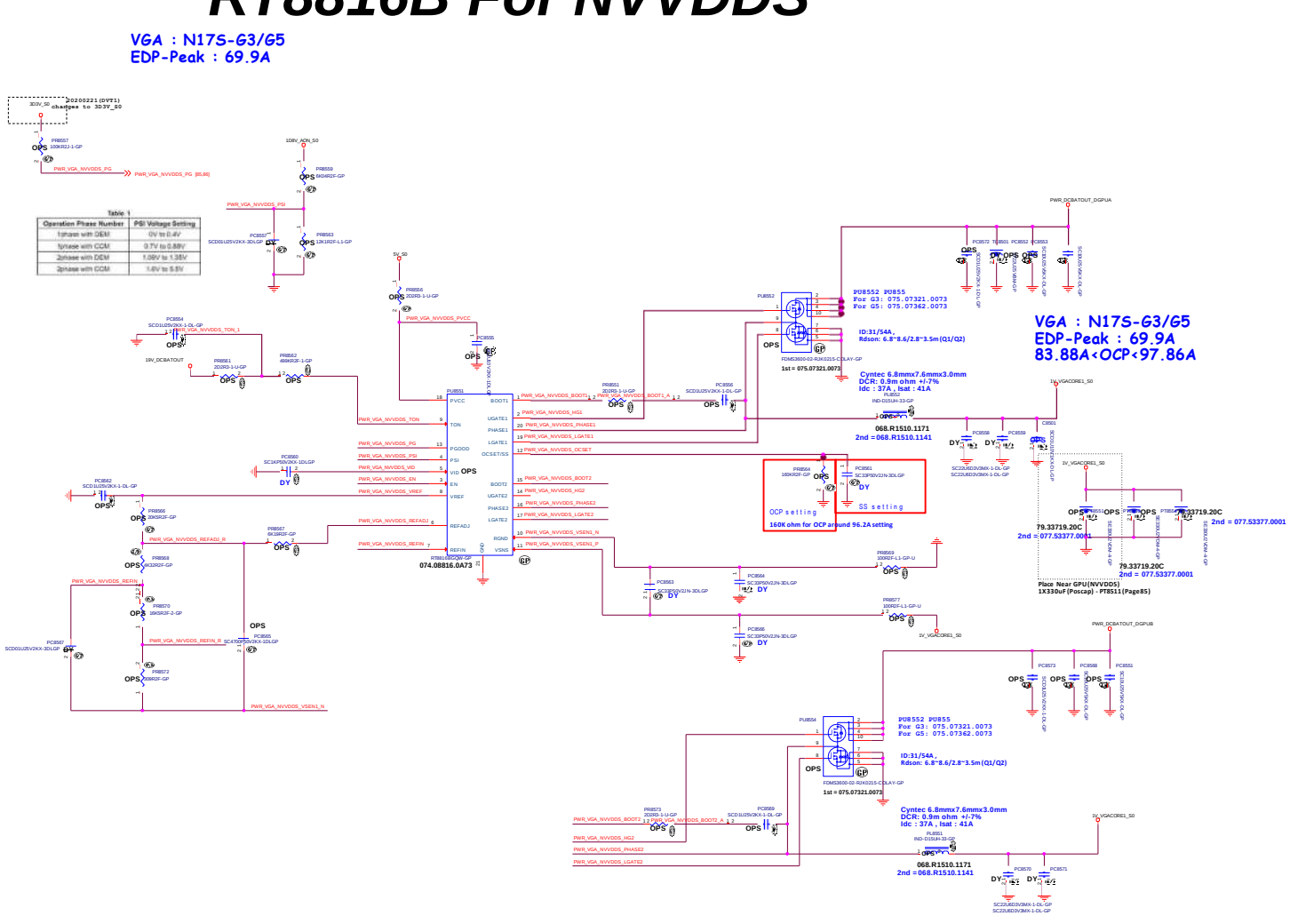
1. Check EE side
2. Modify DAT

PH on EE side

EE need check

For VGA_CORE sequence
EE need check

OFFPAGE-GAP



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GPU (RT8816A_VGA)

Size	Document Number	Rev
A1	HELLCAT_TGL	A00

Date: Saturday, August 08, 2020 Sheet 85 of 105

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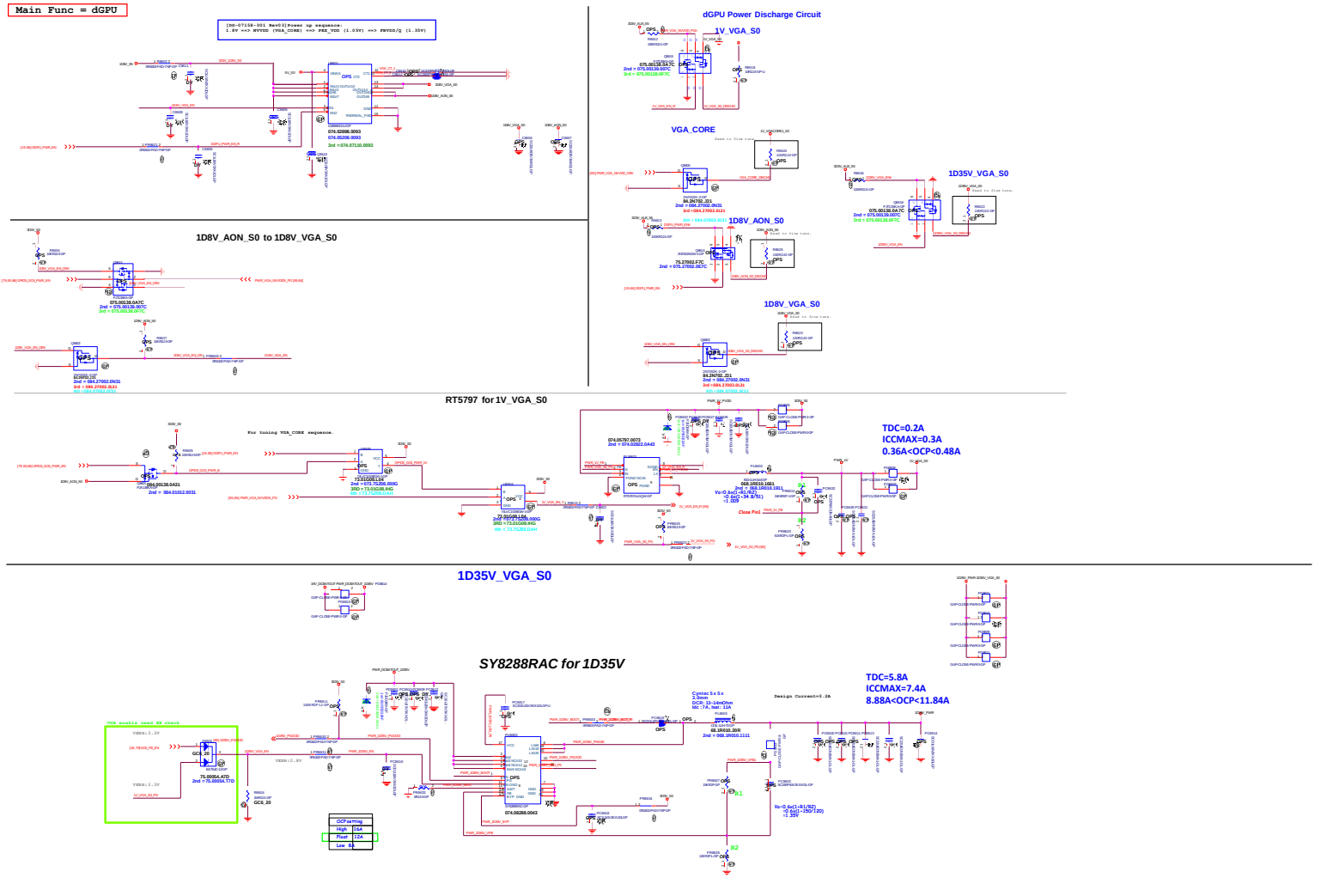


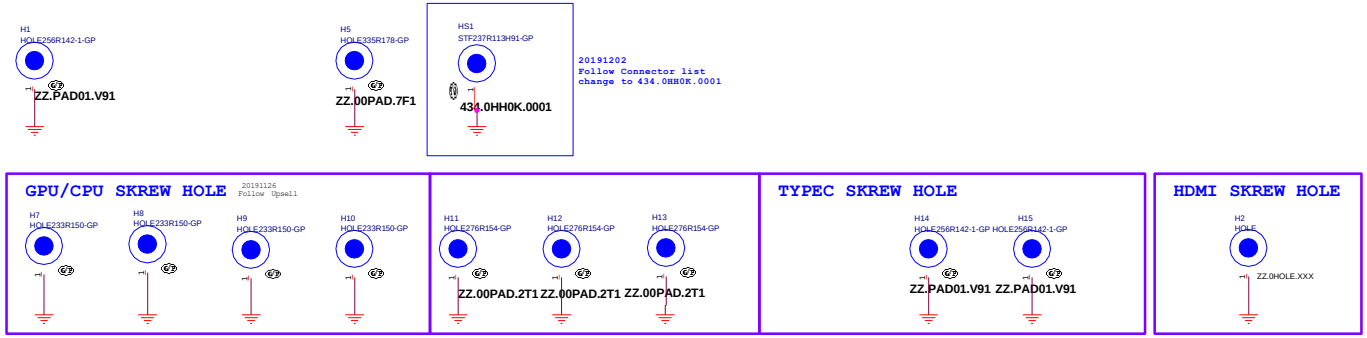
Wistron Corporation

DISCRETE VGA POWER

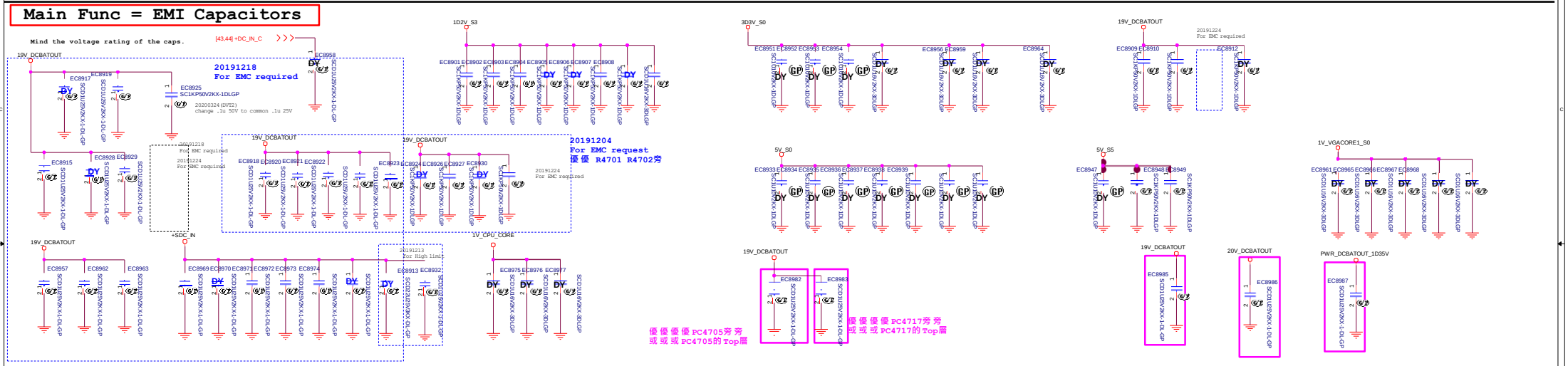
MOCKINGBIRD_TGL

A00

Main Func = UnusedParts



Main Func = EMI Capacitors



Main Func = RF Capacitors

Mind the voltage rating of the caps.

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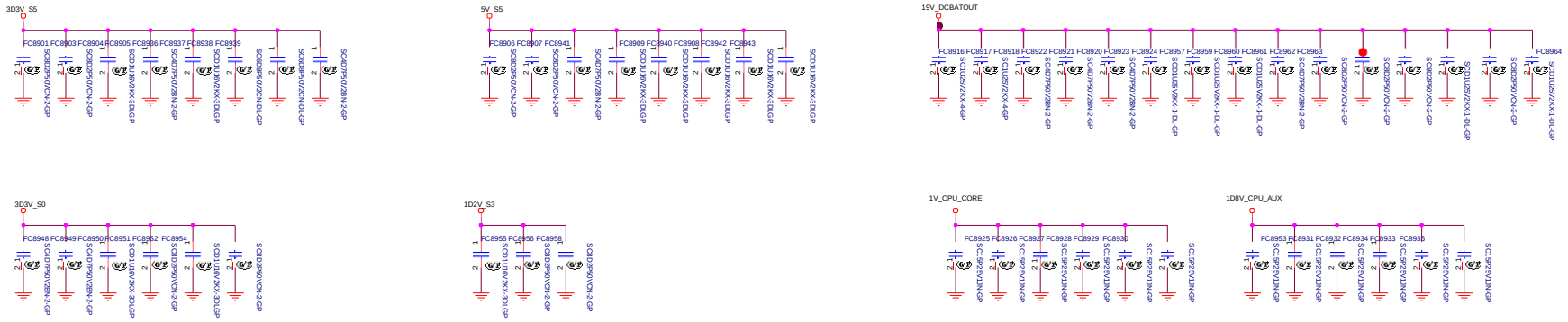

<Core Design>

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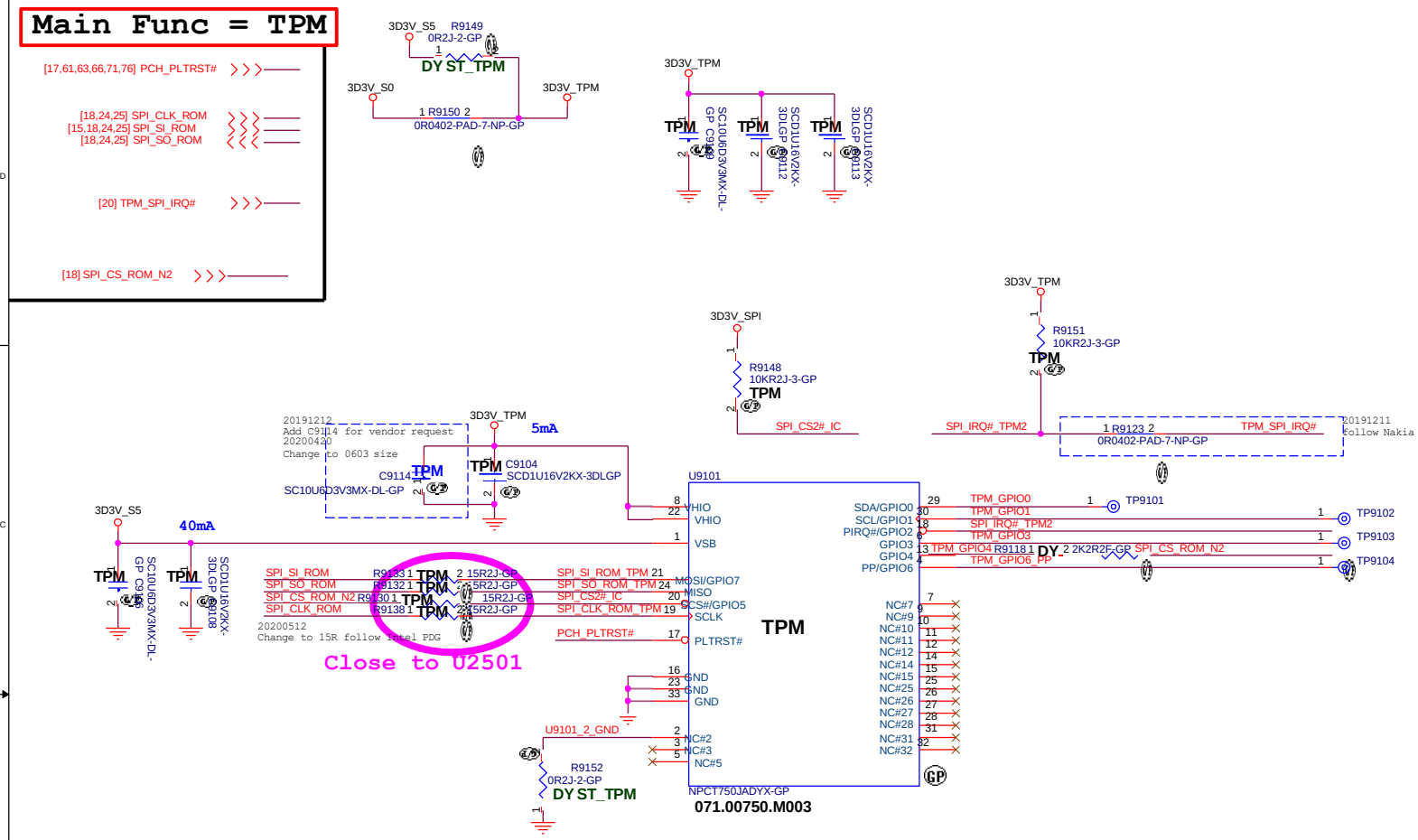
Taipei Hsien 221, Taiwan, R.O.C.

Title: *UNUSED PARTS/EMI Capacitors*

Size	Document Number	Rev
A2	HELLCAT_TGL	A00

Date: Saturday, August 01, 2020 Sheet 89 of 105



<Core Desiign>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***INT IO (TPM)***

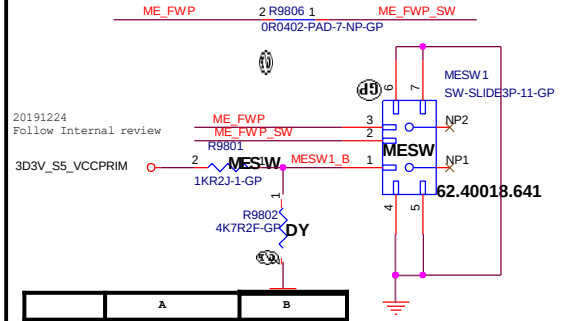
Size	Document Number	Rev
A3	***HELLCAT_TGL***	***A00***

Date: Saturday, August 01, 2020 Sheet 91 of 105

Main Func = Firmware SW

[19] ME_FWP_SW
[24] ME_FWP

Firmware SW



	A	B
ME_FWP	Low	High
	Normal Operation (Default)	Override

	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

<Core Desiign>

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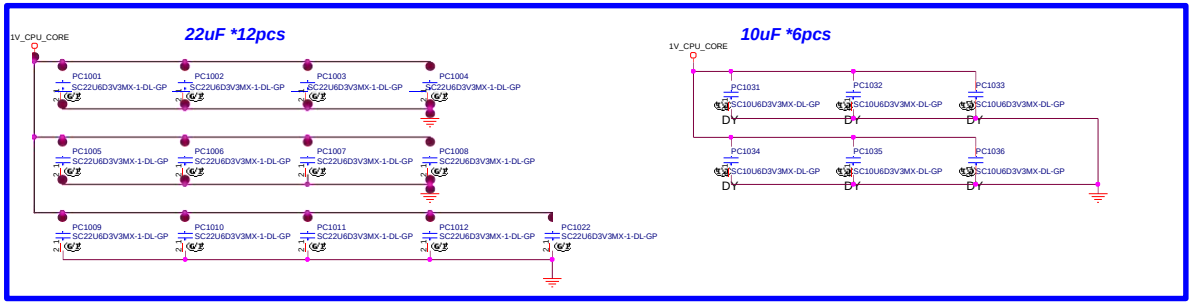
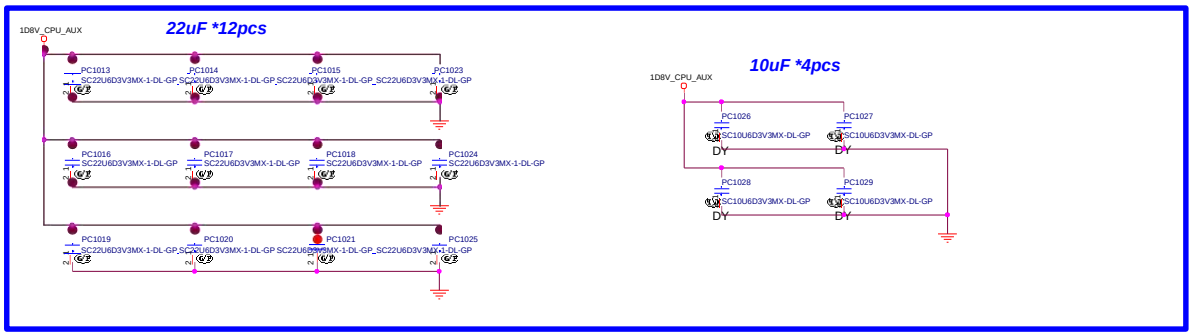
Title: CRT_Switch

Size: A3 | Document Number: HELLCAT_TGL | Rev: A00

Date: Saturday, August 01, 2020 | Sheet 98 of 105

Main Func = CPU





<Core Desiign>

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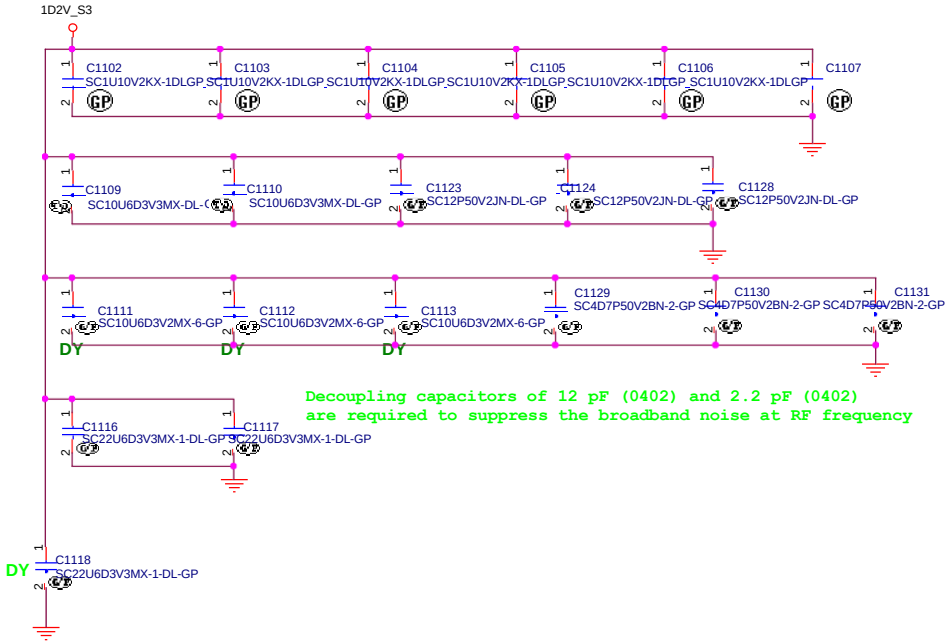
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (CORE Power Cap1)**

Size	Document Number	Rev
A2	HELLCAT_TGL	A00

Date: Saturday, August 01, 2020 Sheet 10 of 105

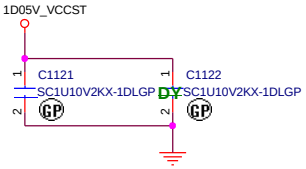
Main Func = CPU

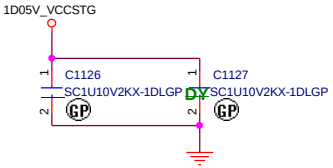


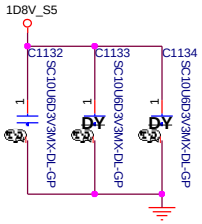
Decoupling Requirements for Ice Lake U Processor for VDDQ

Domain	Backside cap	Primary side cap	Placement guideline [3]
VDDQ	6x 1uF 0402		Place on the back side of the SoC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
	2x 10uF 0402		Place on the back side of the SoC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
	3x 0402 (placeholder)		Place on the back side of the SoC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
	2x 22uF 0603		Place after the TOP DDR signal breakout. These should not be omitted on SODIMM designs, and can be removed only in Memory Down designs when the following conditions are met: 1) DRAM's are soldered down, so their decoupling is shared with the SoC. 2) DRAM's and SoC VDDQ plane copper is shared between both directly (no shorting resistors, pads or similar in the middle). 3) DRAM's are placed close to the SoC allowing that at least 5x10uF capacitors of the DRAM decoupling is within a 30mm radius from SoC Edge.
	1x 0603 (placeholder)		Place after the TOP DDR signal breakout.

Notes:
1. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source.
2. Refer to the Figure 10-10 for decoupling capacitor placements.







11/5 Tery Don
add 1D8V_S5 decoupling cap. follow Shuri

<Core Desiign>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (Power Cap2)**

Size	Document Number	Rev
A3	HELLCAT_TGL	A00

Date: Saturday, August 01, 2020 Sheet 11 of 105

Change notes -

Item #	Subsystem /Component	PHASE	SCH Page #	Change Request Description	Requested By	BOM	Schematic	Layout	Reason of Change
1	EC&KBC&SIO	DVT2	24	Change R2443 to 27K	EE	V			Change Board ID to DVT2
2	PWR.3p3V_5p0V	DVT2	40	Add C4070 & C4071	EE	V	V	V	Follow Vendor's suggestion(add cap to prevent IC broken)
3	GPU.Power	DVT2	86	Add C8613	EE	V	V	V	Follow Vendor's suggestion(add cap to prevent IC broken)
4	Audio.DMIC	DVT2	19	Add U1901, C1901, C1902, R1942, R1943, R1944, R1945, R1946, R1947, R1948 Reserve C1902, R1942	EE	V	V	V	Follow DMIC Vendor's suggestion
5	Conn.WLAN	DVT2	61	Change R6109, R6118 to 49.9 ohm	EE	V			Follow Intel CNVI checklist (575882) change CNV_BRI_RSP and CNV_RGI_RSP damping resistor, from 22 to 49.9 ohm.
6	Platform.BIOS_ROM	DVT2	25	Complete reference plane for SPI signal	EE			V	For reference GND
7	EC&KBC&SIO	DVT2	24	Complete reference plane for eSPI signal	EE			V	For reference GND
8	EC&KBC&SIO	DVT2	24	Change PECI_VREF power to VCCST	EE	V	V	V	Follow Vendor's suggestion
9	IO.Type-C.TBT	DVT2	71	Q7101 , R7178 , R7179 , R7196, R7197 Change to DY	EE	V			Follow Intel TBT check list
10	GPU.Power	DVT2	85	PU8552 , PU8554 Change to 075.07362.0073 for N17s-G5	EE	V			Follow Vendor's suggestion
11	PCH	DVT2	54	premium power circuit stuff for HC15MS	EE	V			premium power circuit for 15MS only